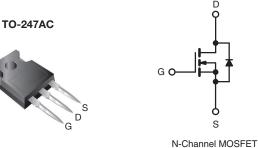


Power MOSFET

PRODUCT SUMMA	RY		
V _{DS} (V)	900		
R _{DS(on)} (Ω)	$V_{GS} = 10 V$	2.5	
Q _g (Max.) (nC)	12	20	
Q _{gs} (nC)	16		
Q _{gd} (nC)	6	7	
Configuration	Sin	gle	



S

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Isolated Central Mounting Hole
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The **TO-247AC** package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220AB devices. The TO-247AC is similar but superior to the earlier TO-218 package because of its isolated mouting hole. It also provides greater creepage distance between pins to meet the requirements of most safety specifications.

ORDERING INFORMATION	
Package	TO-247AC
Lead (Pb)-free	IRFPF40PbF
	SiHFPF40-E3
SnPb	IRFPF40
	SiHFPF40

ABSOLUTE MAXIMUM RATINGS (T $_{\mbox{\scriptsize C}}$	= 25 °C, unl	ess otherwis	se noted)		
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage	Drain-Source Voltage		V _{DS}	900	v
Gate-Source Voltage		V _{GS}	± 20	- V	
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	L	4.7	
	VGS at TO V	T _C = 100 °C	ID	2.9	А
Pulsed Drain Current ^a			I _{DM}	19	
Linear Derating Factor				1.2	W/°C
Single Pulse Avalanche Energy ^b			E _{AS}	500	mJ
Repetitive Avalanche Current ^a			I _{AR}	4.7	A
Repetitive Avalanche Energy ^a			E _{AR}	15	mJ
Maximum Power Dissipation	T _C =	25 °C	PD	150	W
Peak Diode Recovery dV/dt ^c			dV/dt	1.5	V/ns
Operating Junction and Storage Temperature Rang	e		T _J , T _{stg}	- 55 to + 150	- °C
Soldering Recommendations (Peak Temperature) for 10 s			300 ^d		
Mounting Torque	6 22 or 1	//3 screw		10	lbf ∙ in
Mounting Torque	0-32 OF 1	No SCIEW		1.1	N · m

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Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. $V_{DD} = 50 \text{ V}$, starting $T_J = 25 \text{ °C}$, L = 42 mH, $R_g = 25 \Omega$, $I_{AS} = 4.7 \text{ A}$ (see fig. 12). c. $I_{SD} \le 4.7 \text{ A}$, dl/dt $\le 110 \text{ A/}\mu\text{s}$, $V_{DD} \le V_{DS}$, $T_J \le 150 \text{ °C}$. d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

Document Number: 91250 S11-0441-Rev. B, 14-Mar-11 RoHS COMPLIANT

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THERMAL RESISTANCE RATI	NGS							
PARAMETER	SYMBOL	TYP. MAX.			UNIT			
Maximum Junction-to-Ambient	R _{thJA}	- 40			°C/W			
Case-to-Sink, Flat, Greased Surface	R _{thCS}	0.24 -						
Maximum Junction-to-Case (Drain)	R _{thJC}	-		0.83				
SPECIFICATIONS ($T_J = 25 \ ^{\circ}C$,	unless otherw	/ise noted)						
PARAMETER	SYMBOL	TEST	CONDIT	ONS	MIN.	TYP.	MAX.	UNIT
Static								
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0$	V, I _D = 2	50 µA	900	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference t	o 25 °C,	I _D = 1 mA	-	1.0	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_0$	_{GS} , I _D = 2	250 μA	2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _G	$s = \pm 20$	V	-	-	± 100	nA
Zara Cata Valtaga Drain Current		V _{DS} = 90	00 V, V _{GS}	s = 0 V	-	-	100	
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 720 V, V	_{GS} = 0 V	, T _J = 125 °C	-	-	500	μA
Drain-Source On-State Resistance	R _{DS(on)}	$V_{GS} = 10 V$	ار	_D = 2.8 A ^b	-	-	2.5	Ω
Forward Transconductance	9 _{fs}	$V_{DS} = 50 \text{ V}, \text{ I}_{D} = 2.8 \text{ A}^{b}$		2.5	-	-	S	
Dynamic							•	
Input Capacitance	C _{iss}	$V_{GS} = 0 V,$ $V_{DS} = 25 V,$ f = 1.0 MHz, see fig. 5		-	1600	-		
Output Capacitance	C _{oss}			-	180	-	pF	
Reverse Transfer Capacitance	C _{rss}			-	63	-		
Total Gate Charge	Qg				-	-	120	
Gate-Source Charge	Q _{gs}	V _{GS} = 10 V		A, V _{DS} = 360 V, ig. 6 and 13 ^b	-	-	16	nC
Gate-Drain Charge	Q _{gd}		300 1	ig. o and to	-	-	67	
Turn-On Delay Time	t _{d(on)}				-	15	-	
Rise Time	t _r	V _{DD} = 45	0 V I= -	470	-	36	-	
Turn-Off Delay Time	t _{d(off)}	$V_{DD} = 43$ $R_g = 9.1 \Omega, R_f$			-	110	-	ns
Fall Time	t _f				-	32	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from	m		-	5.0	-	
Internal Source Inductance	Ls	package and cer die contact	nter of		-	13	-	nH
Drain-Source Body Diode Characteristic	cs						•	
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the		-	-	4.7	А	
Pulsed Diode Forward Currenta	I _{SM}	integral reverse p - n junction did	ode	a la	-	-	19	
Body Diode Voltage	V_{SD}	T _J = 25 °C, I _S	; = 4.7 A,	$V_{GS} = 0 \ V^{b}$	-	-	1.8	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 4	170 di/	dt – 100 A/ueb	-	510	770	ns
Body Diode Reverse Recovery Charge	Q _{rr}	$r_{\rm J} = 20$ 0, $r_{\rm F} = 2$., A, Ul/	αι – 100 Αγμο-	-	2.2	3.3	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-	on time	is negligible (turn	-on is doi	minated b	y L _S and	L _D)

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width \leq 300 µs; duty cycle \leq 2 %.

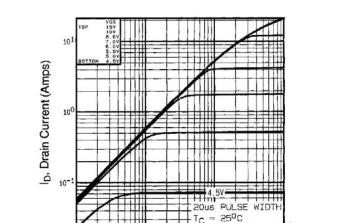
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10-1

IRFPF40, SiHFPF40

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

 V_{DS} , Drain-to-Source Voltage (volts) Fig. 1 - Typical Output Characteristics, T_C = 25 °C

101

102

100

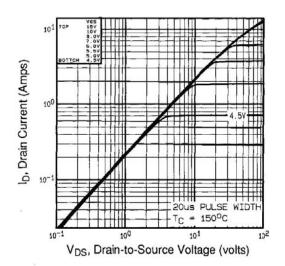


Fig. 2 - Typical Output Characteristics, $T_C = 150$ °C

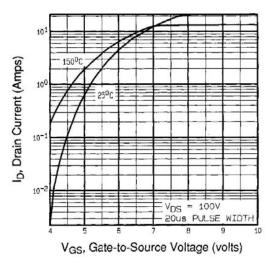


Fig. 3 - Typical Transfer Characteristics

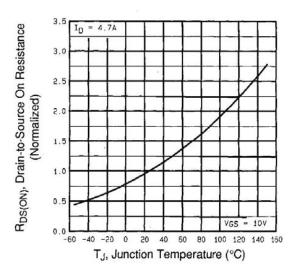


Fig. 4 - Normalized On-Resistance vs. Temperature

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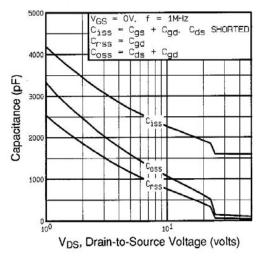


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

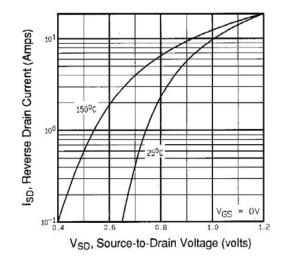


Fig. 7 - Typical Source-Drain Diode Forward Voltage

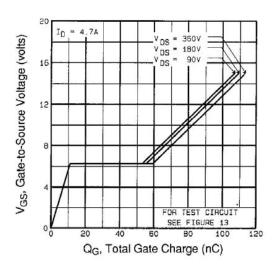


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

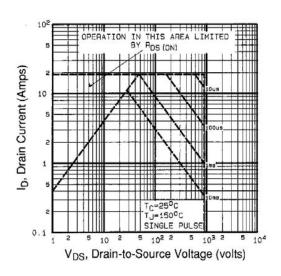


Fig. 8 - Maximum Safe Operating Area

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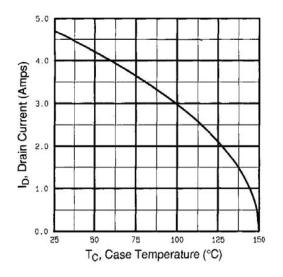


Fig. 9 - Maximum Drain Current vs. Case Temperature

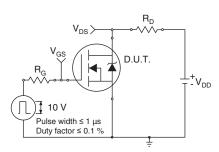


Fig. 10a - Switching Time Test Circuit

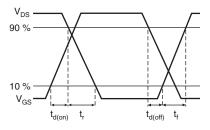


Fig. 10b - Switching Time Waveforms

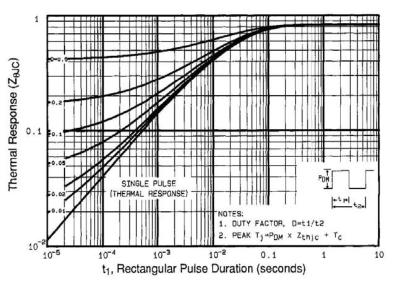


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

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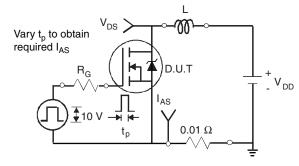


Fig. 12a - Unclamped Inductive Test Circuit

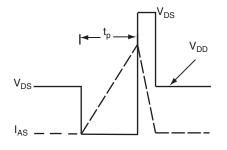


Fig. 12b - Unclamped Inductive Waveforms

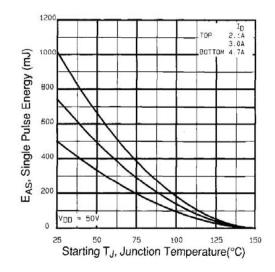
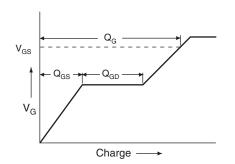


Fig. 12c - Maximum Avalanche Energy vs. Drain Current





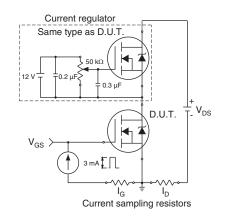
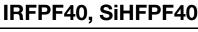


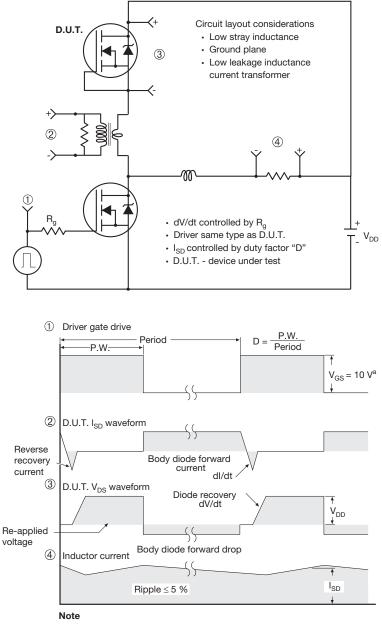
Fig. 13b - Gate Charge Test Circuit

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Peak Diode Recovery dV/dt Test Circuit



a. V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

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TO-247AC (High Voltage)

VERSION 1: FACILITY CODE = 9





Section C--C, D--D, E--E

	MILLIN	IETERS	
DIM.	MIN.	MAX.	NOTES
А	4.83	5.21	
A1	2.29	2.55	
A2	1.50	2.49	
b	1.12	1.33	
b1	1.12	1.28	
b2	1.91	2.39	6
b3	1.91	2.34	
b4	2.87	3.22	6, 8
b5	2.87	3.18	
С	0.55	0.69	6
c1	0.55	0.65	
D	20.40	20.70	4

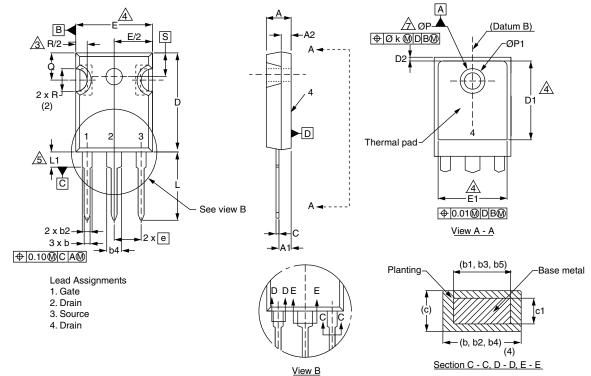
	MILLIN	IETERS	
DIM.	MIN.	MAX.	NOTES
D1	16.25	16.85	5
D2	0.56	0.76	
E	15.50	15.87	4
E1	13.46	14.16	5
E2	4.52	5.49	3
е	5.44	BSC	
L	14.90	15.40	
L1	3.96	4.16	6
ØP	3.56	3.65	7
Ø P1	7.19) ref.	
Q	5.31	5.69	
S	5.54	5.74	

Notes

- ⁽¹⁾ Package reference: JEDEC[®] TO247, variation AC
- (2) All dimensions are in mm
- ⁽³⁾ Slot required, notch may be rounded
- ⁽⁴⁾ Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
- ⁽⁵⁾ Thermal pad contour optional with dimensions D1 and E1
- (6) Lead finish uncontrolled in L1
- (7) Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
- (8) Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition



VERSION 2: FACILITY CODE = Y



	MILLIN	IETERS	
DIM.	MIN.	MAX.	NOTES
A	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
С	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	-	

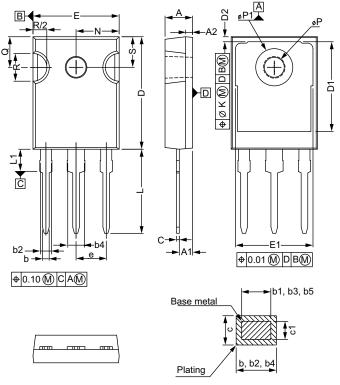
	MILLIN	IETERS	
DIM.	MIN.	MAX.	NOTES
D2	0.51	1.30	
E	15.29	15.87	
E1	13.72	-	
е	5.46	BSC	
Øk	0.2	254	
L	14.20	16.25	
L1	3.71	4.29	
ØΡ	3.51	3.66	
Ø P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51	BSC	

Notes

- ⁽¹⁾ Dimensioning and tolerancing per ASME Y14.5M-1994
- ⁽²⁾ Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- ⁽⁴⁾ Thermal pad contour optional with dimensions D1 and E1
- ⁽⁵⁾ Lead finish uncontrolled in L1
- ⁽⁶⁾ Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
- ⁽⁷⁾ Outline conforms to JEDEC outline TO-247 with exception of dimension c



VERSION 3: FACILITY CODE = N



	MILLIN	IETERS		MILLIN	IETERS
DIM.	MIN.	MAX.	DIM.	MIN.	MAX.
А	4.65	5.31	D2	0.51	1.35
A1	2.21	2.59	E	15.29	15.87
A2	1.17	1.37	E1	13.46	-
b	0.99	1.40	е	5.46	BSC
b1	0.99	1.35	k	0.:	254
b2	1.65	2.39	L	14.20	16.10
b3	1.65	2.34	L1	3.71	4.29
b4	2.59	3.43	N	7.62	BSC
b5	2.59	3.38	Р	3.56	3.66
С	0.38	0.89	P1	-	7.39
c1	0.38	0.84	Q	5.31	5.69
D	19.71	20.70	R	4.52	5.49
D1	13.08	-	S	5.51	BSC

Notes

⁽¹⁾ Dimensioning and tolerancing per ASME Y14.5M-1994

⁽²⁾ Contour of slot optional

(3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body

⁽⁴⁾ Thermal pad contour optional with dimensions D1 and E1

⁽⁵⁾ Lead finish uncontrolled in L1

⁽⁶⁾ Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")



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