Application Note AN-41

# PeakSwitch®
## Design Guide

## Introduction

The *PeakSwitch* family is a highly integrated, monolithic, off-line switcher IC designed for use in power supplies that have to deliver peak loads for short durations. Example applications include inkjet printers, audio amplifiers and DVRs. When peak power is required, the effective switching frequency can approach 277 kHz, allowing a transformer with a small core size to be used. Innovative proprietary features, such as adaptive switching cycle on-time control, adaptive current limit, AC line sense and fast AC reset greatly simplify the design. This reduces engineering design time and system cost while providing complete system-level protection and robust functionality.

Each member of the family has a high-voltage power MOSFET and its controller integrated onto the same die. Internal start-up bias current is drawn from a high-voltage current source connected to the DRAIN pin, eliminating the need for external start-up components. The internal oscillator is frequency modulated (jitter) to reduce EMI. In addition, the ICs have integrated functions that provide system-level protection. The auto-restart function limits the dissipation in the MOSFET, the transformer and the output diode during overload, output short-circuit and open-loop conditions, while the auto-recovering hysteretic thermal shutdown function disables MOSFET switching during a thermal fault. On-time extension enables more power to be delivered at low line and extends hold-up time. The smart AC line sense and undervoltage lockout (UVLO) functions enable the IC to latch off whenever a fault activates the auto-restart function, and to be reset quickly after AC power is removed.

Power Integrations' *EcoSmart*® technology enables supplies designed around the *PeakSwitch* family members to consume <300 mW of no-load power and to meet harmonized energy efficiency standards such as the California Energy Commission (CEC), EU and ENERGY STAR.

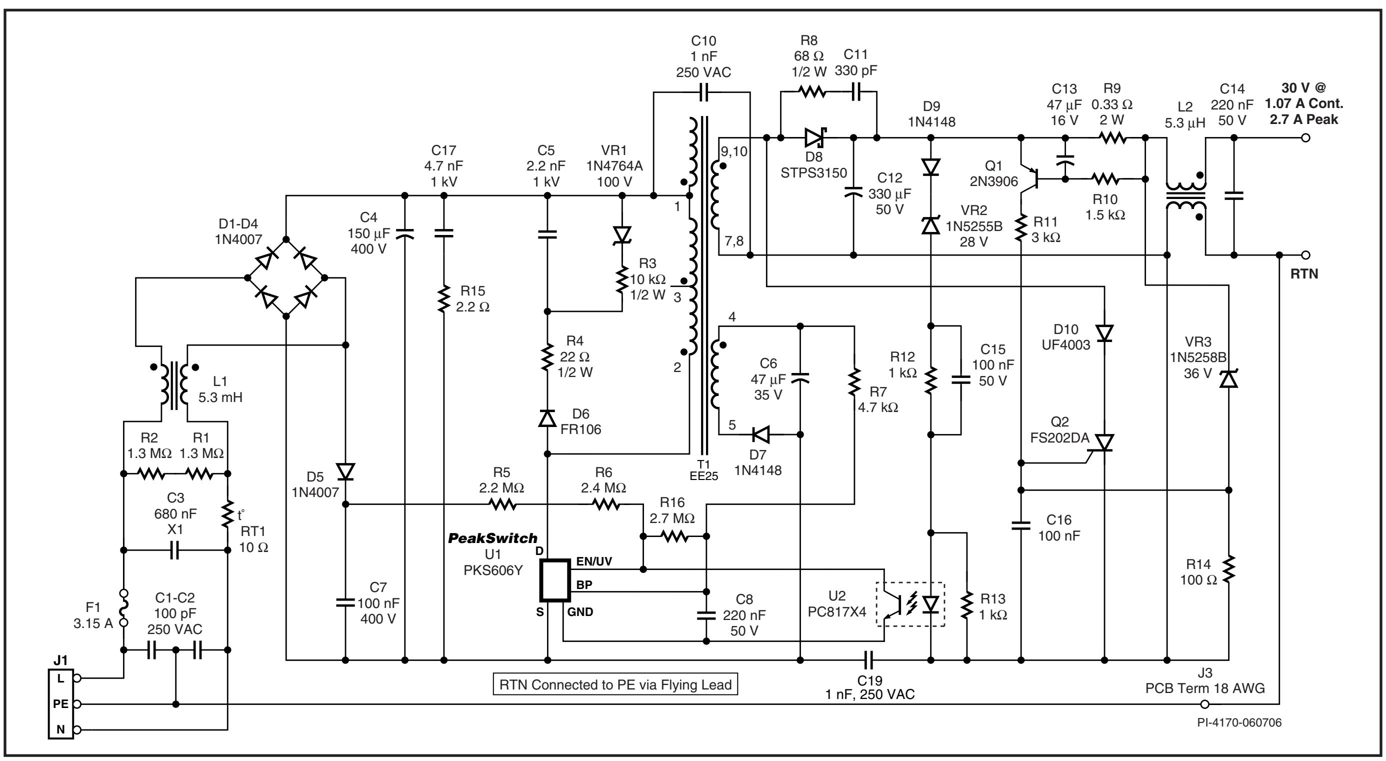



*Figure 1. PeakSwitch PKS606Y, 32 W Average, 81 W Peak, Universal Input Power Supply.*

## Scope

This application note is intended for engineers designing an isolated AC-DC flyback power supply using the *PeakSwitch* family of devices. It provides guidelines to enable the engineer to quickly select key components and also complete a suitable transformer design. To simplify the task, this application note refers directly to the *PI Xls* design spreadsheet that is part of the *PI Expert*™ power supply design software suite.

In addition to this application note, the reader may also find the *PeakSwitch* Reference Design Kit (RDK) (the RDK contains an engineering prototype board, engineering report and device sample) useful as an example of a working power supply. Further details on downloading *PI Expert*, obtaining an RDK and updates to this document can be found at www.powerint.com.

**Quick Start**

Readers can use the following information to quickly design a transformer and select the components for a first prototype. Only the information described below needs to be entered into the *PI Xls* spreadsheet; other parameters will be automatically selected by the spreadsheet, based on a typical design. References to spreadsheet cell locations are provided in square brackets [cell reference].

- Enter AC input voltage range $VAC_{MIN}$, $VAC_{MAX}$ and minimum line frequency $f_L$ [B3, B4, B5]
- Enter nominal output voltage $V_O$ [B6]
- Enter minimum output voltage at peak load assuming an output drop is acceptable (if applicable) [B7]
- Enter maximum output current at peak load or maximum continuous load as applicable [B5]
- Enter continuous (average) output power [B9]
- Enter efficiency estimate:

  0.7 for universal input voltage (85-265 VAC) or single 100/115 VAC (85-132 VAC) line voltage, and 0.75 for single 230 VAC (185-265 VAC) line voltage designs. Adjust the efficiency estimate accordingly, after measuring the efficiency of the first prototype-board at peak load and $VAC_{MIN}$. [B11]

- Enter loss allocation factor Z [B12]:

  0.65 for typical application (adjust the number accordingly after first proto-board evaluation)

- Enter $C_{IN}$ input capacitance [B14]:

  Use 2 $\mu F/W_{PK}$ for universal (85-265 VAC) or single (100/115 VAC) line voltage, if output voltage droop is acceptable, or 3 $\mu F/W_{PK}$ if output voltage droop is unacceptable.

  Use 1 $\mu F/W_{PK}$ single 230 VAC for a single (185-265 VAC) high-line voltage.

- Select *PeakSwitch* from drop down list or enter directly [B17]:

Select the device in the table below according to output power and line input voltage.

| OUTPUT POWER TABLE | | | | |
|---|---|---|---|---|
| PRODUCT[3] | 230 VAC ±15% | | 85-265 VAC | |
| | Adapter Cont.[1] | Adapter Peak[2] | Adapter Cont.[1] | Adapter Peak[2] |
| PKS603 P | 13 W | 32 W | 9 W | 25 W |
| PKS604 P | 23 W | 56 W | 16 W | 44 W |
| PKS604 Y/F | 35 W | 56 W | 23 W | 44 W |
| PKS605 P | 31 W | 60 W | 21 W | 44 W |
| PKS605 Y/F | 46 W | 79 W | 30 W | 58 W |
| PKS606 P | 35 W | 66 W | 25 W | 46 W |
| PKS606 Y/F | 68 W | 117 W | 45 W | 86 W |
| PKS607 Y/F | 75 W | 126 W | 50 W | 93 W |

*Table 1. Output Power Table (See Data Sheet for Notes 1, 2 and 3).*

- Enter $V_D$ – forward voltage drop of the output diode [B25]:

  0.5 V for Schottky diode
  0.7 V for PN diode

- Enter core type (if desired) from drop down menu [B43]:

A suggested core size will be selected automatically by the spreadsheet if none is entered.

- Build transformer
- Select key components (see Steps 5 through 10)
- Build prototype, test and iterate the design as necessary, entering measured values into the spreadsheet where estimates were initially used (e.g. efficiency, $V_{MIN}$)

# Step-by-Step Transformer Design Procedure

## Introduction

*PeakSwitch* devices have current limit values that allow the supply to deliver the specified peak power given in the power table. With sufficient heatsinking, these power levels could be provided continuously. However, *PeakSwitch* is optimized for use in applications that demand short duration, high peak power, while delivering a significantly lower continuous power. Typical peak-to-continuous ratios would be $P_{PEAK} \geq 2 \times P_{AVE}$. The high switching frequency of *PeakSwitch* allows a small core size to deliver the peak power but the short duration prevents the transformer windings from overheating and reduces heatsinking requirement for the device.

As the average power increases, based on the measured transformer temperature, it may be necessary to select a larger transformer so that the current density of its windings can be decreased.

The power table provides some guidance for peak and continuous (average) power levels in sealed adapters, although specific applications may vary. For example, if the peak power condition is of very low duty cycle, such as a two-second peak occurring at power up to accelerate a hard disk drive, then the temperature rise of the transformer is a function of the continuous power. However, if the peak power occurs every 200 ms for 50 ms, then peak power heating effects would need to be considered.

Figure 2 shows how to calculate the average power requirements for a design with two different peak load conditions.

$$P_{AVE} = P_1 + (P_3 - P_1) \cdot \delta_1 + (P_2 - P_1) \cdot \delta_2$$

$$\delta_1 = \frac{\Delta t_1}{T}, \delta_2 = \frac{\Delta t_2}{T}$$

Where $P_x$ represents the different output power conditions, $\Delta t_x$ represent the durations of each peak power condition and T is the period of one cycle of the pulsed load condition.

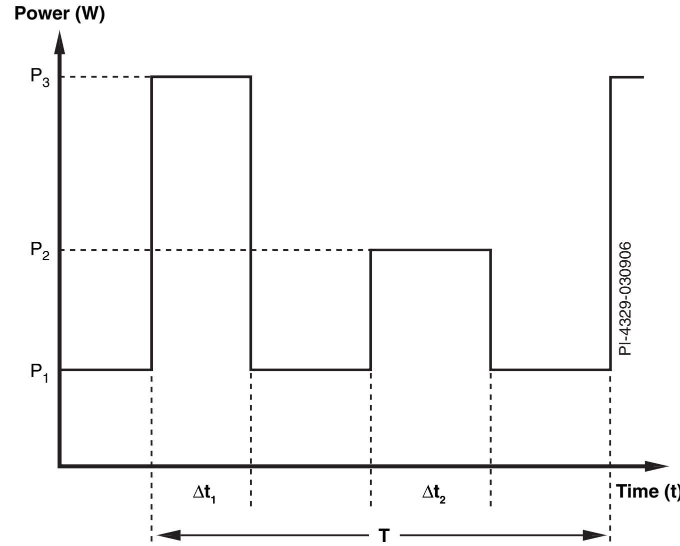



*Figure 2. Continuous (Average) Output Power Calculation Example.*

The design procedure requires both peak and continuous powers to be specified. The peak power is used to select the *PeakSwitch* device and design the transformer for power delivery at minimum input line voltage while continuous power (or average power if the peak load is periodic) is used for thermal design and may affect the size of the transformer and the heat sink.

### Step 1. Enter Application Variables $VAC_{MIN}$, $VAC_{MAX}$, $f_L$, $V_O$, $I_O$, $V_O$ at Peak Load, $\eta$, Z, $t_C$, $C_{IN}$

Determine the input voltage range from Table 2.

| Nominal Input Voltage (VAC) | $VAC_{MIN}$ | $VAC_{MAX}$ |
|---|---|---|
| 100/115 | 85 | 132 |
| 230 | 195 | 265 |
| Universal | 85 | 265 |

*Table 2. Standard Worldwide Input Line Voltage Ranges.*

| ENTER APPLICATION VARIABLES | | | | | AN41 Example |
|---|---|---|---|---|---|
| VACMIN | 85 | | | Volts | Minimum AC Input Voltage |
| VACMAX | 265 | | | Volts | Maximum AC Input Voltage |
| fL | 50 | | | Hertz | AC Mains Frequency |
| Nominal Output Voltage (VO) | 24.00 | | | Volts | Nominal Output Voltage (at continuous power) |
| Maximum Output Current (IO) | 0.75 | | | Amps | Power Supply Output Current (corresponding to peak power) |
| Minimum Output Voltage at Peak Load | | | 24.00 | Volts | Minimum Output Voltage at Peak Power (Assuming output droop during peak load) |
| Continuous Power | 6.00 | | 6.00 | Watts | Continuous Output Power |
| Peak Power | | | 18.00 | Watts | Peak Output Power |
| n | 0.70 | | | | Efficiency Estimate at output terminals and at peak load. Enter 0.7 if no better data available |
| Z | | | 0.60 | | Loss Allocation Factor (Z = Secondary side losses / Total losses) |
| tC Estimate | 3.00 | | | mSeconds | Bridge Rectifier Conduction Time Estimate |
| CIN | 47.00 | | 47 | uFarads | Input Capacitance |

*Figure 3. Application Variable Section of PeakSwitch Design Spreadsheet.*

**Line Frequency, $f_L$**
47 Hz for universal or 100/115 VAC input. 47 Hz for single 230 VAC input. For half-wave rectification use $f_L/2$. For DC input enter the voltage directly into Cells B55 and B56.

**Nominal Output Voltage, $V_O$ (V)**
Enter the nominal output voltage of the main output during the continuous load condition. Generally, the main output is the output from which feedback is derived.

**Output Current, $I_O$ (A)**
Enter the maximum output current under peak load conditions. If the design does not have a peak load condition, then enter the maximum continuous output current. In multiple output designs, the output current of the main output (typically, the output from which feedback is taken) should be increased such that the peak power (or maximum continuous power as applicable) matches the sum of the output powers from all of the supply's outputs. The individual output voltages and currents should then be entered at the bottom of the spreadsheet [cells B98 to B131].

**Minimum Output Voltage at Peak Load (V)**
The output voltage may be specified in *PeakSwitch* designs based on whether or not the output voltage is allowed to droop during peak loads. If the application requires the output to remain the same under continuous and peak load conditions, leave this cell empty. The spreadsheet then assumes that the output voltage under peak load conditions is equal to the nominal output voltage, i.e. the output is not allowed to droop under peak load.

If the application allows the output voltage to droop under peak load conditions, enter the minimum acceptable voltage at peak load. The peak power is then calculated based on the output current and the minimum acceptable output voltage. In multiple output designs, if the main output is allowed to droop then all the other output voltages will also droop proportionally under peak load conditions.

**Continuous Output Power (W)**
Enter the continuous output power. If this entry is left blank the design spreadsheet assumes that the continuous power is equal to the peak output power. This value is used by the spreadsheet to suggest a core size.

**Peak Power (W)**
This is a calculated value based on the minimum output voltage at peak load, and maximum output current. It is used to calculate the required value of the primary inductance.

**Power Supply Efficiency, $\eta$**
Enter the estimated efficiency of the complete power supply, measured at the output terminals under peak load conditions and worst-case line (generally lowest input voltage). Start with a value of 0.7 (typical) for a design where the majority of the output power is drawn from an output voltage of 12 V or greater, and no current sensing is present on the secondary. Once a prototype has been constructed, the measured efficiency should be entered and the design of the transformer should be iterated.

**Power Supply Loss Allocation Factor, Z**
This factor represents the proportion of losses between the primary and the secondary of the power supply. Z factor is used together with the efficiency number, to determine the actual power that must be delivered by the power stage. For example, losses in the input stage (EMI filter, rectification, etc) are not processed by the power stage (transferred through the transformer), and therefore, although they reduce efficiency, the transformer design is not impacted.

$$Z = \frac{Secondary\ Side\ Losses}{Total\ Losses}$$

For designs that do not have a secondary current sense circuit, enter 0.65. For those designs that do have a secondary current sense circuit, use a value of 0.7 until measurements can be made on a prototype. The higher number indicates larger secondary side losses associated with the secondary side current sense resistor.

**Bridge Diode Conduction Time, $t_C$ (ms)**
Enter a bridge diode conduction time of 3.75 ms, if there is no better data available.

**Total Input Capacitance, $C_{IN}$ (μF)**
Enter the total input capacitance, using Table 3 for guidance.

| | **Total Input Capacitance per Watt Output Power (μF/W)** |
|---|---|
| AC Input Voltage (VAC) | Full Wave Rectification |
| 100/115 | 3 |
| 230 | 1 |
| 85-265 | 3 |

*Table 3. Suggested Total Input Capacitance for Different Input Voltage Ranges.*

The capacitance is used to calculate the minimum DC voltage and should be selected to keep the minimum DC input voltage ($V_{MIN}$) >70 V.

For designs that have a DC rather than an AC input, the value of the minimum and maximum DC input voltages, $V_{MIN}$ and $V_{MAX}$, may be entered directly into the override cells on the design spreadsheet shown below.

| DC INPUT VOLTAGE PARAMETERS | | | | | |
|---|---|---|---|---|---|
| VMIN | | | 80 | Volts | Minimum DC Input Voltage |
| VMAX | | | 375 | Volts | Maximum DC Input Voltage |

*Figure 4. DC Input Voltage Parameters Showing Grey Override Cells for DC Input Designs.*

## Step 2 – Enter *PeakSwitch* Variables: *PeakSwitch* Device, $V_{OR}$, $V_{DS}$, $V_D$, $V_{DB}$, $V_{CLO}$, $K_{P(STEADY\ STATE)}$, $K_{P(TRANSIENT)}$

**Select the correct *PeakSwitch* device**

Refer to Table 1 and first select a device based on the peak output power of the design. Then compare the continuous power rating to the continuous numbers in the power table. If the continuous power exceeds the value given in the power table, then the next largest device should be selected. Similarly, if the continuous power is close to the power table's power levels, then it may be necessary to switch to a larger device based on the measured thermal performance of the prototype.

3. Higher $V_{OR}$ increases the leakage inductance of the transformer, which reduces efficiency of the power supply.
4. Higher $V_{OR}$ increases the peak and RMS currents on the secondary side, which may increase secondary side copper and diode losses.

Optimal selection of the $V_{OR}$ value should be based on a reasonable engineering compromise of the factors mentioned above.

**PeakSwitch On-State Drain to Source Voltage, $V_{DS}$ (V)**

This parameter is the average on-state voltage developed across

| ENTER PeakSwitch VARIABLES | | | | | |
|---|---|---|---|---|---|
| **PeakSwitch** | **PKS603P** | | **PKS603P** | | PeakSwitch device |
| *Chosen Device* | | *PKS603P* | | | |
| ILIMITMIN | | | 0.750 | Amps | Minimum Current Limit |
| ILIMITMAX | | | 0.870 | Amps | Maximum Current Limit |
| fSmin | | | 250000 | Hertz | Minimum Device Switching Frequency |
| I^2fmin | | | 164 | A^2kHz | I^2f (product of current limit squared and frequency is trimmed for tighter tolerance) |
| VOR | | | 110 | Volts | Reflected Output Voltage (VOR <= 135 V Recommended) |
| VDS | | | 10 | Volts | PeakSwitch on-state Drain to Source Voltage |
| VD | | | 0.7 | Volts | Output Winding Diode Forward Voltage Drop |
| VDB | | | 0.7 | Volts | Bias Winding Diode Forward Voltage Drop |
| VCLO | | | 200 | Volts | Nominal Clamp Voltage |
| KP (STEADY STATE) | | | 0.60 | | Ripple to Peak Current Ratio (KP < 6) |
| KP (TRANSIENT) | | | 0.38 | | Ripple to Peak Current Ratio under worst case at peak load (0.25 < KP < 6) |

*Figure 5. PeakSwitch Section of Design Spreadsheet.*

**Peak Load Switching Frequency, $f_{s(min)}$ (Hz)**

This parameter is the worst-case minimum switching frequency based on the minimum data sheet value of $I^2f$ (not adjustable).

**Reflected Output Voltage, $V_{OR}$ (V)**

This parameter is the secondary winding voltage during the diode conduction time, which is reflected back to the primary through the turns ratio of the transformer. The default value is 110 V, however the acceptable range for $V_{OR}$ is between 80 V and 135 V, providing that no warnings are produced by the spreadsheet. For design optimization purposes, the following should be kept in mind:

1. Higher $V_{OR}$ allows increased power delivery at $V_{MIN}$, which minimizes the value of the input capacitor and the droop of the output voltage when the on-time extension feature is used, and maximizes the power delivery from a given *PeakSwitch* device.
2. Higher $V_{OR}$ reduces the voltage stress on the output diodes, which in some cases may allow a Schottky diode to be used, and will thus give higher efficiency.

the DRAIN and SOURCE pins of the *PeakSwitch* device. By default, if the grey override cell is left empty, a value of 10 V is assumed for Y/F package devices, and 5 V for P package devices. Use the default value if no better data is available.

**Output Diode Forward Voltage Drop, $V_D$ (V)**

Enter the average forward voltage drop of the (main) output diode. Use 0.5 V for a Schottky diode or 0.7 V for a PN diode, if no better data is available. The spreadsheet uses a default value of 0.7 V.

**Nominal Clamp Voltage, $V_{CLO}$ (V)**

Enter the nominal clamp voltage. The clamp is used to ensure that maximum voltage developed across the DRAIN and SOURCE pins of the internal MOSFET remains below the $BV_{DSS}$ specification (700 V) limit, with sufficient margin. It is recommended that a Zener diode with a value of 200 V be used in the clamp circuit. Even if an RCD clamp is used, a Zener should be placed in parallel with the RCD circuit to provide hard clamping during fault conditions. By default, if the grey override cell is left empty, a value of 200 V is assumed, which is also the maximum value recommended. Lower values can be used, as the $V_{OR}$ is reduced from 135 V, and/or in designs with low effective (primary and reflected secondary) leakage inductance values.

**Ripple to Peak Current Ratio, $K_{P(STEADYSTATE)}$ and $K_{P(TRANSIENT)}$**
Below a value of 1, indicating continuous conduction mode, $K_P$ is the ratio of ripple to peak primary current (Figure 6).

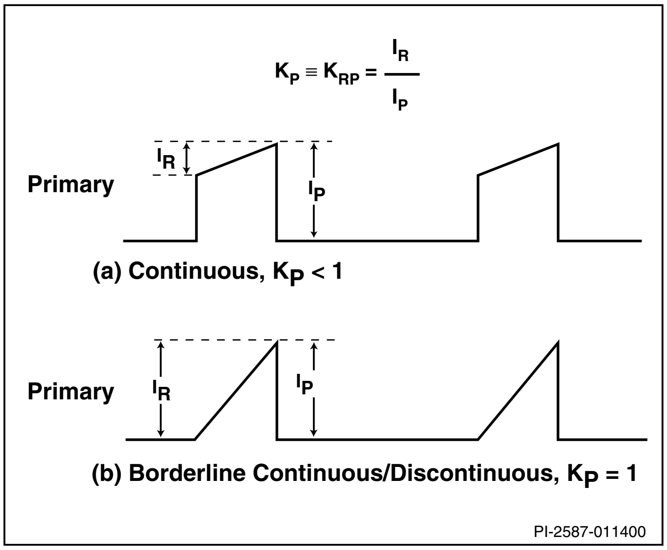



*Figure 6. Continuous Mode Current Waveform, $K_P \leq 1$.*

$$K_P \equiv K_{RP} = \frac{I_R}{I_P}$$

Above a value of 1, indicating discontinuous conduction mode, $K_P$ is the ratio of primary MOSFET off time to the secondary diode conduction time.

$$K_P \equiv K_{DP} = \frac{(1-D)\times T}{t}$$
$$= \frac{V_{OR}\times(1-D_{MAX})}{(V_{MIN}-V_{DS})\times D_{MAX}}$$

The value of $K_P$ should be in the range of $0.25 < K_P < 6$ and guidance is given in the comments cell if the value is outside this range.

$K_{P\,(STEADY\,STATE)}$ is the calculated $K_P$ value under the condition where several switching cycles have occurred consecutively.

$K_{P\,(TRANSIENT)}$ is the calculated minimum $K_P$ value that occurs after a switching cycle has been skipped. When the drain current starts from zero and ramps to the current limit, the on time for this first cycle is much longer than during steady state operation. This reduces the off time, reducing the time for the magnetizing inductance to reset, and causing the next cycle to start with a much higher initial current, a lower ripple current and a lower value of $K_P$.

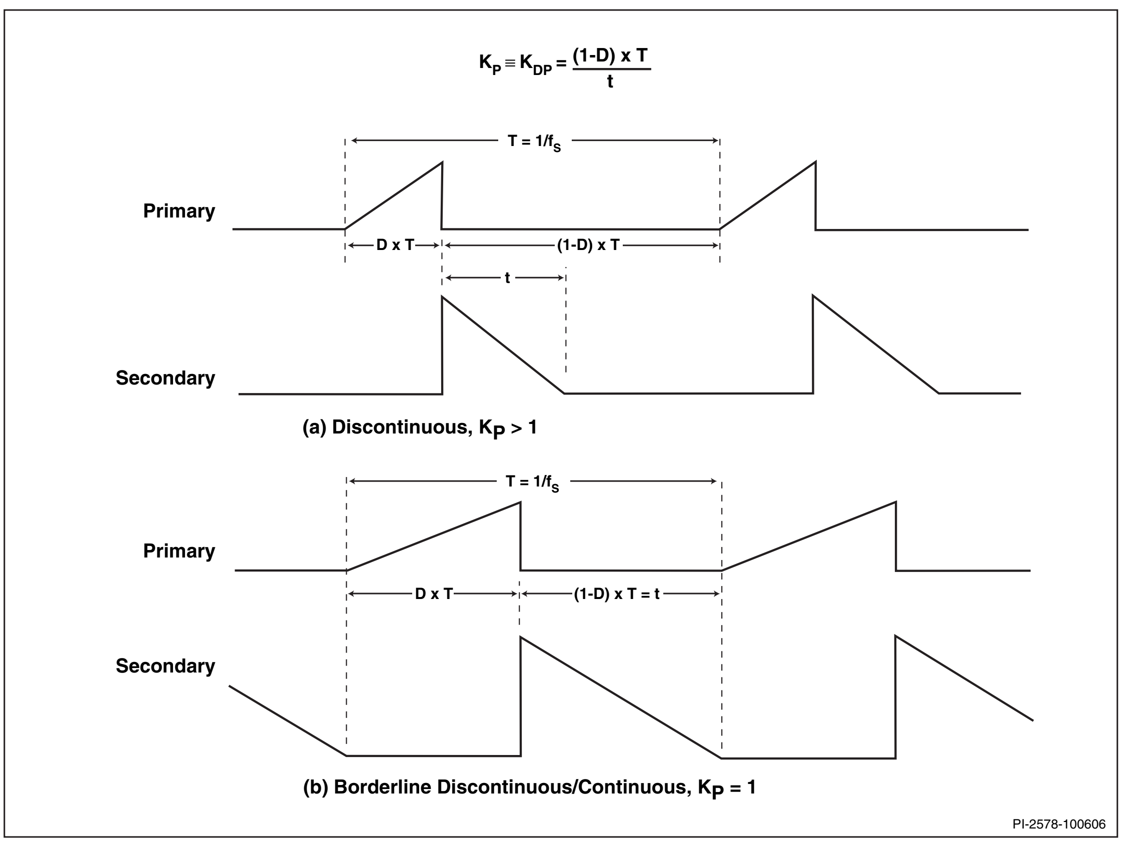



*Figure 7. Discontinuous Mode Current Waveform, $K_P \geq 1$.*

Figure 8 provides an illustration of the difference between transient and steady state $K_P$. It shows a series of drain current waveforms for a design that does not meet $K_{P\ (TRANSIENT)}$ limits.

In region (a) the $K_P$ is stable with a value of 0.38. In region (b) the control loop has caused a switching cycle to be skipped, allowing the flux in the transformer core to be completely reset as the output diode is allowed to conduct for a much longer duration than in region (a). On the next switching cycle (c), the feedback loop has enabled a switching pulse and the current ramps from zero rather than some initial value. This means that the on-time for switching cycle (c) is much longer than for (a), allowing less off-time (the time during which the output diode conducts), yielding less resetting of the core flux. Therefore, cycle (d) starts with a much larger initial current pedestal than during the steady state conditions of (a). In the following cycles, (e) and (f), the value of $K_P$ settles again to the $K_{P\ (STEADY\ STATE)}$ of 0.38.

The sequence of skipped cycle (b) followed by a cycle that gives the minimum possible off time (c) is where the spreadsheet calculates the value of $K_{P(TRANSIENT)}$. In this example, $K_{P\ (TRANSIENT)}$ is 0.19, below the 0.25 limit and is thus unacceptable. To address this problem a larger device could be selected, the $V_{OR}$ increased, or the output power reduced.

$K_{P(TRANSIENT)}$ should be above a value of 0.25 to prevent the large initial current pedestal from falsely triggering current limit at the end of the leading edge blanking time and limiting power delivery. Similar guidance is given in the comment cell on how to maintain $K_{P\ (TRANSIENT)}$ within acceptable limits.

### Step 3 – Enter Under-Voltage Lock Out (UVLO) Variables, $V_{\_UV\_TARGET}$ (V)

The line under-voltage lockout feature of *PeakSwitch* sets the minimum startup voltage of the supply, prevents the power supply output from glitching when the input voltage is below the normal operating range, and is used to determine if the supply should latch off during a fault. Connecting a resistor from an input capacitor to the EN/UV pin enables this feature. Enter the desired DC voltage across the input capacitor, at which the power supply should start operating. The spreadsheet calculates both the ideal resistor value and closest standard value, together with the typical start-up voltage based on the closest standard value (Figure 9). Either a resistor with a voltage rating >375 V or two series resistors whose voltage rating sum is >375 V should be used.

### Step 4 – Choose Bias Winding Output Voltage, $V_B$ (V)

By default, if the grey override cell is left empty, a value of 15 V is assumed. The user can override this value as needed. However, the value should be in the range of 8 V $<V_B$ <20 V. The lower value ensures adequate headroom for supplying current into the BYPASS pin. The upper value limits the no-load input power consumption caused by high power consumption in the bias winding. The number of bias winding turns, $N_B$, is to be used for transformer construction. An ultra-fast diode with a voltage rating above the calculated PIVB value should be selected. Select the value of resistor from the bias supply to the BYPASS pin to provide the maximum data sheet supply current for the selected *PeakSwitch* device.

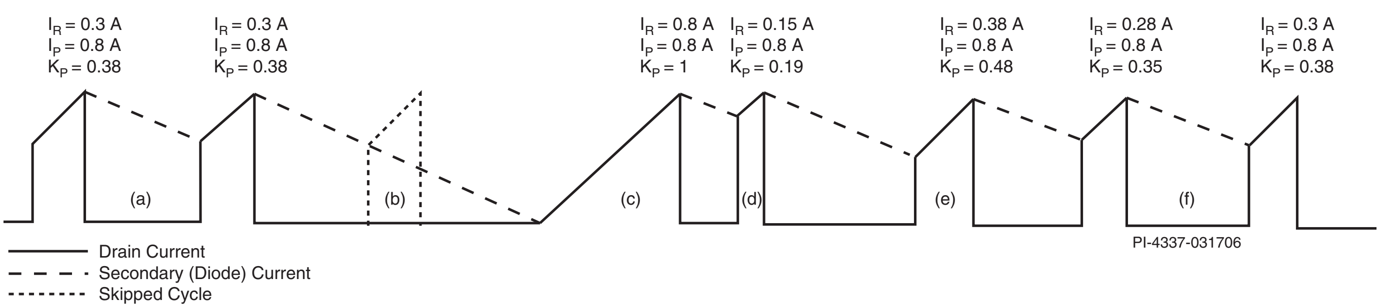



*Figure 8. Drain Current Waveform Illustrating $K_{P(STEADY\ STATE)}$ and $K_{P(TRANSIENT)}$.*

| ENTER UVLO VARIABLES | | | | | |
|---|---|---|---|---|---|
| V_UV_TARGET | | | 88 | Volts | Target DC under-voltage threshold, above which the power supply with start |
| V_UV_ACTUAL | | | 85 | Volts | Typical DC start-up voltage based on standard value of RUV_ACTUAL |
| RUV_IDEAL | | | 3.45 | Mohms | Calculated value for UV Lockout resistor |
| RUV_ACTUAL | | | 3.30 | Mohms | Closest standard value of resistor to RUV_IDEAL |

*Figure 9. Under-Voltage Variables Section of Design Spreadsheet.*

| BIAS WINDING VARIABLES | | | | | |
|---|---|---|---|---|---|
| VB | | | 15.00 | Volts | Bias winding Voltage |
| NB | | | 10 | | Number of Bias Winding Turns |
| PIVB | | | 68 | Volts | Bias rectifier Maximum Peak Inverse Voltage |

*Figure 10. Bias Winding Variables Section of Design Spreadsheet.*

## Step 5 – Choose Core and Bobbin Based on Output Power, and Enter $A_E$, $L_E$, $A_L$, BW, M, L, $N_S$

Core effective cross-sectional area, $A_E$: ($cm^2$)
Core effective path length, $L_E$: (cm).
Core ungapped effective inductance, $A_L$: (nH/turn$^2$).
Bobbin width, BW: (mm)
Tape margin width equal to half the total margin, M (mm)
Primary Layers, L
Secondary Turns, $N_S$

| ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES | | | | | |
|---|---|---|---|---|---|
| **Core Type** | **Auto** | | **EE13** | | Transformer Core (Verify acceptable thermal rise under continuous load conditions) |
| *Core* | | *EE13* | | *P/N:* | PC40EE13-Z |
| *Bobbin* | | *EE13_BOBBIN* | | *P/N:* | EE13_BOBBIN |
| AE | | | 0.171 | cm^2 | Core Effective Cross Sectional Area |
| LE | | | 3.02 | cm | Core Effective Path Length |
| AL | | | 1130 | nH/T^2 | Ungapped Core Effective Inductance |
| BW | | | 7.90 | mm | Bobbin Physical Winding Width |
| M | | | 0.00 | mm | Safety Margin Width (Half the Primary to Secondary Creepage Distance) |
| L | | | 3 | | Number of Primary Layers |
| NS | | | 16 | | Number of Secondary Turns |

*Figure 11. Transformer Variables Section of Design Spreadsheet.*

### Core Type
By default if the core type cell is left empty, the spreadsheet will select the smallest commonly available core suitable for the continuous output power. Available cores can be selected from the drop down list in the tool bar of the *PI Xls* design software. The grey override cells can be used to enter the core and bobbin parameter directly by a user. This is useful if the user wants to use a core that is not on the list, or the specific core or bobbin information differs from that recalled by the spreadsheet.

### Safety Margin, M (mm)
For designs that require isolation but are not using triple insulated wire, the width of the safety margin to be used on each side of the bobbin should be entered here. For universal input designs, a total margin of 6.2 mm would be required, and a value of 3.1 mm would be entered into the spreadsheet. For vertical bobbins, the margin may not be symmetrical. However if a total margin of 6.2 mm were required, then 3.1 mm would still be entered even if the physical margin is only on one side of the bobbin.

For designs using triple insulated wire, it may still be necessary to enter a small margin in order to meet the required safety creepage distances. Many bobbins exist for each core size, and each will have different mechanical spacing. Refer to the specific bobbin data sheet or seek guidance from your safety expert or transformer vendor to determine what specific margin is required.

Since margin construction reduces the available area for the windings, it may not be suitable for small core sizes. If after entering the margin, more than three primary layers (L) are required, either a larger core should be selected, or consider a zero margin design using triple insulated wire.

### Primary Layers, L
By default, if the override cell is empty, a value of 3 is assumed. Primary layers should be in the range of $1 < L < 3$ and in general it should be the lowest number that meets the primary current density limit of 100 Cmils/Amp (CMA). More than three layers are possible, but the increased leakage inductance and physical fit of the windings should be considered. Due to the high switching frequency of *PeakSwitch* designs, it is important to minimize transformer leakage inductance. Therefore split primary construction is recommended for all designs regardless of power level. In split primary construction, half of the primary winding is placed on either side of the secondary and bias windings, in a sandwich arrangement.

### Secondary Turns, $N_S$
By default, if the grey override cell is left blank, the minimum number of secondary turns is calculated such that the maximum operating flux density $B_M$ is kept below the recommended maximum of 3000 Gauss (300 mT). In general it is not necessary to enter a number in the override cell except in designs where a lower operating flux density is desired (see the explanation of $B_M$ limits).

## Step 6 – Iterate Transformer Design and Generate Initial Design

Iterate the design making sure that no warnings are displayed. Any parameters outside the recommended range of values can be corrected by following the guidance given in the right hand column.

Once all warnings have been cleared, the output transformer design parameters can be used to either wind a prototype transformer or sent to a vendor for samples.

The key transformer electrical parameters are:

### Primary Inductance, $L_P$ (μH)
This is the target nominal primary inductance of the transformer.

**Primary Inductance Tolerance, $L_{P\_TOLERANCE}$(%)**
This is the assumed primary inductance tolerance. A value of 12% is used by default. However, if specific information is known from the transformer vendor, then this may be entered in the grey override cell.

**Number of Primary Turns, $N_P$**
Total number of primary turns. For low leakage inductance it is recommended that split primary construction be used.

Gapped core effective inductance, $A_{LG}$ ($nH/T^2$) used by the transformer vendor to specify the core gap.

**Target $B_M$ (Gauss)**
The value entered here is used to calculate the number of secondary turns. By default, a value of 2800 Guass is used, slightly below the recommended maximum $B_M$ value of 3000 Gauss. This accounts for the rounding down of the number of calculated secondary turns in some designs.

**Maximum Operating Flux Density, $B_M$ (Gauss)**
A maximum value of 3000 Gauss during normal operation is recommended to limit the maximum flux density under start up and output short circuit. Under these conditions, the output voltage is low and little reset of the transformer occurs during the MOSFET off time. This may allow the transformer flux density to staircase above the normal operating level. A value of 3000 Gauss at the peak current limit of the selected device, together with the built-in protection features of *PeakSwitch* provides sufficient margin to prevent core saturation under startup or output short circuit conditions.

The cycle skipping mode of operation used in *PeakSwitch* can produce audio frequency displacements in the transformer. To limit this noise, the transformer should be designed such that the peak core flux density is below 3000 Gauss (300 mT). Following this guideline and using the standard transformer production technique of dip varnishing practically eliminates audible noise. A careful evaluation of the audible noise performance should be made, using production transformer samples before approving the design. When ceramic capacitors that have Z5U dielectrics are used in clamp circuits, they too may produce audible sound. They should be replaced with capacitors that have a different dielectric, such as polyester film.

**Maximum Primary Wire Diameter, OD (mm)**
By default, if the override cell is empty, double coated wire is assumed and a standard wire diameter is chosen. The grey override cells can be used to enter a wire diameter directly.

Primary wire size, DIA: (mm)
Primary wire gauge, AWG
Number of primary layers, L
Estimated core center leg gap length: $L_g$: (mm)
Number of secondary turns, $N_S$
Secondary wire size, $DIA_S$: (mm)
Secondary wire gauge, $AWG_S$

In multiple output designs $N_{Sx}$, $CM_{Sx}$, $AWG_{Sx}$ (where x is the output number) should also be used.

| TRANSFORMER PRIMARY DESIGN PARAMETERS | | | | | |
|---|---|---|---|---|---|
| LP | | | 367 | uHenries | Typical Primary Inductance. +/- 12% to ensure a minimum primary inductance of 328 uH |
| LP_TOLERANCE | | | 12 | % | Primary inductance tolerance |
| NP | | | 71 | | Primary Winding Number of Turns |
| ALG | | | 72 | nH/T^2 | Gapped Core Effective Inductance |
| Target BM | | | 2800 | Gauss | Target Peak Flux Density at Maximum Current Limit |
| BM | | | 2624 | Gauss | Calculated Maximum Operating Flux Density, BM < 3000 is recommended |
| BAC | | | 789 | Gauss | AC Flux Density for Core Loss Curves (0.5 X Peak to Peak) |
| ur | | | 1588 | | Relative Permeability of Ungapped Core |
| LG | | | 0.28 | mm | Gap Length (Lg > 0.1 mm) |
| BWE | | | 23.7 | mm | Effective Bobbin Width |
| OD | | | 0.33 | mm | Maximum Primary Wire Diameter including insulation |
| INS | | | 0.06 | mm | Estimated Total Insulation Thickness (= 2 * film thickness) |
| DIA | | | 0.28 | mm | Bare conductor diameter |
| AWG | | | 30 | AWG | Primary Wire Gauge (Rounded to next smaller standard AWG value) |
| CM | | | 102 | Cmils | Bare conductor effective area in circular mils |
| CMA | | | 208 | Cmils/Amp | Primary Winding Current Capacity (100 < CMA < 500) |

*Figure 12. Transformer Primary Design Section of Design Spreadsheet.*

| TRANSFORMER SECONDARY DESIGN PARAMETERS | | | | | |
|---|---|---|---|---|---|
| **Lumped parameters** | | | | | |
| ISP | | | 3.34 | Amps | Peak Secondary Current |
| ISRMS | | | 1.74 | Amps | Secondary RMS Current |
| IRIPPLE | | | 1.57 | Amps | Output Capacitor RMS Ripple Current |
| CMS | | | 349 | Cmils | Secondary Bare Conductor minimum circular mils |
| AWGS | | | 24 | AWG | Secondary Wire Gauge (Rounded up to next larger standard AWG value) |

*Figure 13. Transformer Secondary Primary Parameters Section of Design Spreadsheet – Lumped into Single Output.*

| TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS) | | | | | |
|---|---|---|---|---|---|
| **1st output** | | | | | |
| VO1 | | | 24 | Volts | Main Output Voltage (if unused, defaults to single output design) |
| IO1 | | | 0.750 | Amps | Output DC Current |
| PO1 | | | 18.00 | Watts | Output Power |
| VD1 | | | 0.7 | Volts | Output Diode Forward Voltage Drop |
| NS1 | | | 16.00 | | Output Winding Number of Turns |
| ISRMS1 | | | 1.744 | Amps | Output Winding RMS Current |
| IRIPPLE1 | | | 1.57 | Amps | Output Capacitor RMS Ripple Current |
| PIVS1 | | | 108 | Volts | Output Rectifier Maximum Peak Inverse Voltage |
| Recommended Diodes | | | **BYV27-200** | | Recommended Diodes for this output |
| CMS1 | | | 349 | Cmils | Output Winding Bare Conductor minimum circular mils |
| AWGS1 | | | 24 | AWG | Wire Gauge (Rounded up to next larger standard AWG value) |
| DIAS1 | | | 0.51 | mm | Minimum Bare Conductor Diameter |
| ODS1 | | | 0.49 | mm | Maximum Outside Diameter for Triple Insulated Wire |
| **2nd output** | | | | | |
| VO2 | | | | Volts | Output Voltage |
| IO2 | | | | Amps | Output DC Current |
| PO2 | | | 0.00 | Watts | Output Power |
| VD2 | | | 0.7 | Volts | Output Diode Forward Voltage Drop |
| NS2 | | | 0.45 | | Output Winding Number of Turns |
| ISRMS2 | | | 0.000 | Amps | Output Winding RMS Current |
| IRIPPLE2 | | | 0.00 | Amps | Output Capacitor RMS Ripple Current |
| PIVS2 | | | 2 | Volts | Output Rectifier Maximum Peak Inverse Voltage |
| Recommended Diode | | | | | Recommended Diodes for this output |
| CMS2 | | | 0 | Cmils | Output Winding Bare Conductor minimum circular mils |
| AWGS2 | | | N/A | AWG | Wire Gauge (Rounded up to next larger standard AWG value) |
| DIAS2 | | | N/A | mm | Minimum Bare Conductor Diameter |
| ODS2 | | | N/A | mm | Maximum Outside Diameter for Triple Insulated Wire |
| **3rd output** | | | | | |
| VO3 | | | | Volts | Output Voltage |
| IO3 | | | | Amps | Output DC Current |
| PO3 | | | 0.00 | Watts | Output Power |
| VD3 | | | 0.7 | Volts | Output Diode Forward Voltage Drop |
| NS3 | | | 0.45 | | Output Winding Number of Turns |
| ISRMS3 | | | 0.000 | Amps | Output Winding RMS Current |
| IRIPPLE3 | | | 0.00 | Amps | Output Capacitor RMS Ripple Current |
| PIVS3 | | | 2 | Volts | Output Rectifier Maximum Peak Inverse Voltage |
| Recommended Diode | | | | | Recommended Diodes for this output |
| CMS3 | | | 0 | Cmils | Output Winding Bare Conductor minimum circular mils |
| AWGS3 | | | N/A | AWG | Wire Gauge (Rounded up to next larger standard AWG value) |
| DIAS3 | | | N/A | mm | Minimum Bare Conductor Diameter |
| ODS3 | | | N/A | mm | Maximum Outside Diameter for Triple Insulated Wire |
| | | | | | |
| **Total power** | | | 18 | Watts | Total Output Power |
| | | | | | |
| Negative Output | | | N/A | | If negative output exists enter Output number; eg: If VO2 is negative output, enter 2 |

*Figure 14. Transformer Secondary Design Parameters Section of Spreadsheet – Multiple Outputs.*

## Step 7 – Selection of *PeakSwitch* External Components

### Bypass Pin Capacitor

For the BYPASS pin, use a 0.33 µF, 50 V ceramic capacitor or a 1 µF, 50 V electrolytic, whichever is lower cost.

## Step 8 – Selection of Under-Voltage or AC Line Sense Components

UVLO prevents the supply from starting up prematurely, while latching shutdown protects the IC, the supply and the load from fault conditions. The rectified AC input voltage that forces the current into the EN/UV pin to exceed 25 µA sets the UVLO threshold.

For example, if regulation is lost due to a short circuit, an open loop or an output overload condition, and the input voltage is sufficient to support normal operation (>25 µA into the EN/UV pin), then *PeakSwitch* will latch off. To reset the latch, the AC input has to be removed long enough so that the current into the EN/UV pin falls below the 25 µA UV threshold. Once AC is reapplied, the next time the EN/UV pin current exceeds 25 µA, the supply will attempt to restart.

For some applications, the time for the EN/UV pin current to fall below 25 µA may be excessive due to the time for the bulk input capacitor to discharge. In such cases, a fast AC reset circuit can be used allowing latching shutdown to be independent of the load and voltage on the bulk input capacitor. This prevents race conditions that could cause unwanted triggering during brownout or on removal of the AC input.

Referring to Figure 1, the fast AC reset circuit is comprised of D5, C7, R5 and R6. The incoming AC is rectified by D5 and filtered by C7 with R5 and R6 providing the line sensing current into the EN/UV pin. When AC power is removed (after a fault has occurred and the unit has latched off), C7 discharges quickly via R5 and R6. The value of C7 is selected so that the current through R5 and R6 has fallen below the UV threshold (25 µA) after the desired reset time (~3 seconds as shown) has elapsed. The capacitor should have a voltage rating greater than $VAC_{MAX} \times \sqrt{2}$, with 400 V metal film capacitors being a suitable choice.

If the line UVLO function and latching shutdown are desired and fast AC reset is not required, then the resistor value from step 3 can be connected from the UV/EN pin to the positive side of the input bulk capacitor.

If no resistors are fitted then the *PeakSwitch* device senses this condition and the UVLO function is disabled.

The sense resistor should be rated above 400 V, generally requiring either a single 0.5 W resistor or two 0.25 W resistors connected in series.

### Step 9 – Selection of Primary Clamp Components

It is recommended that either a Zener clamp or an RCD combined with a Zener clamp be used in *PeakSwitch* designs. This is to ensure that the peak drain voltage is limited to below the $BV_{DSS}$ of the internal MOSFET while still maximizing efficiency and minimizing no-load consumption.

A standard RCD clamp designed to limit the peak drain voltage under peak load conditions represents a significant load as the output power is reduced, resulting in low light load efficiency and high no-load consumption.

Figure 1 shows an example of an optimized clamp arrangement. The addition of VR1 in series with R3 prevents C5 from discharging below 100 V as the effective switching frequency lowers as the load is reduced. The value of R3 is selected so that the peak drain voltage is limited to an acceptable level under worst-case conditions of maximum input voltage, maximum ambient temperature and maximum overload power or a short circuit on the output of the supply.

The peak drain voltage should be limited to a maximum voltage of 650 V under these conditions to provide margin for component variation. In the sample design shown in these steps, the peak drain voltage was limited to 600 V. The clamp diode (D6) must

| Series Number | Type | $V_R$ Range | $I_D$ | Package | Manufacturer |
|---|---|---|---|---|---|
| | | V | A | | |
| IN5817 to 1N5819 | Schottky | 20-40 | 1 | Leaded | Vishay |
| SB120 to SB1100 | Schottky | 20-100 | 1 | Leaded | Vishay/Fairchild |
| 11DQ50 to 11DQ60 | Schottky | 50-60 | 1 | Leaded | IR |
| 1N5820 to 1N5822 | Schottky | 20-40 | 3 | Leaded | Vishay |
| MBR320 to MBR360 | Schottky | 20-60 | 3 | Leaded | IR/On Semi |
| SS12 to SS16 | Schottky | 20-60 | 1 | SMD | Vishay |
| SS32 to SS36 | Schottky | 20-60 | 3 | SMD | Vishay |
| SB540 to SB560 | Schottky | 40-60 | 5 | Leaded | Vishay |
| UF4002 to UF4006 | Ultrafast | 100-600 | 1 | Leaded | Vishay |
| MUR110 to MUR160 | Ultrafast | 100-600 | 1 | Leaded | On Semi |
| UF5401 to UF5408 | Ultrafast | 100-800 | 3 | Leaded | Vishay |
| ES1A to ES1D | Ultrafast | 50-200 | 1 | SMD | Vishay |
| ES2A to ES2D | Ultrafast | 50-200 | 2 | SMD | Vishay |
| BYV28-200 | Ultrafast | 200 | 3.5 | Leaded | Vishay |
| MBR745 to MBR760 | Schottky | 40-60 | 7.5 | TO220 | Vishay |
| MBR1045 to MBR10100 | Schottky | 45-100 | 10 | TO220 | Vishay |
| BYW29-100 to BYW29-200 | Ultrafast | 100-200 | 8 | TO220 | Vishay |

*Table 4. List of Diodes Suitable For Use as the Output Rectifier.*

be a fast or an ultra-fast recovery type with a reverse recovery time <500 ns. Under no circumstances should a slow recovery rectifier diode be used. The high dissipation that may result during startup or an output short circuit can cause failure of the diode. Resistor R4 dampens ringing for reduced EMI.

Supplies using different devices in the *PeakSwitch* family will have different peak primary current, leakage inductances and leakage energy. Therefore, C5 and R3 should be optimized for each design. As a general rule, minimize the value of capacitor C5 and maximize the value of resistor R3.

### Step 10 – Select Output Rectifier Diode

For each output, use the values of peak inverse voltage ($V_R$) and output current ($I_O$) provided in the design spreadsheet to select the output diodes. Table 4 shows some commonly available types.

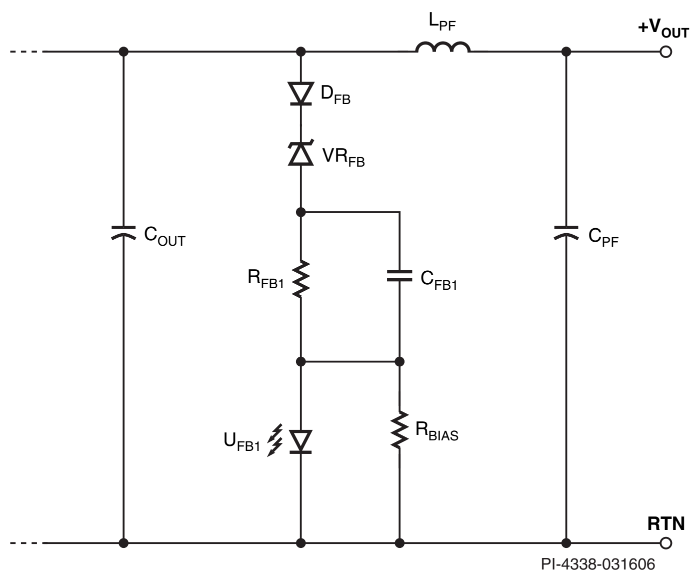
$V_R \geq 1.25 \times$ PIVS: where PIVS is taken from the *Voltage Stress Parameters* section of the spreadsheet and *Transformer Secondary Design Parameters (Multiple Outputs)*.

$I_D \geq 2 \times I_O$: where $I_D$ is the rated DC current of the diode and $I_O$ is the average output current. Depending on the thermal rise and duration of the peak load condition, it may be necessary to increase the diode current rating once a prototype has been built. This also applies to the amount of heatsinking required.

### Step 11 – Select Output Capacitor

**Ripple Current Rating**

The spreadsheet calculates the output capacitor ripple current at peak load. Therefore the actual rating of the capacitor will depend on the peak to average power ratio of the design. For a conservative design, select the output capacitor(s) such that the ripple rating is greater than the calculated value, $I_{RIPPLE}$ from the spreadsheet, calculated at the peak load condition. However in designs with high peak to continuous (average) power ratios, the capacitor rating can be reduced based on the measured temperature rise under worst-case load and ambient temperature. If a suitable individual capacitor cannot be found, then two or more capacitors may be used in parallel to achieve a combined ripple current rating equal to the sum of the individual capacitor ratings.




<table>
<tr><th>Output Voltage (V)</th><th>Zener Value, $VR_{FB}$ (V)</th><th>Feedback Bias Resistor, $R_{BIAS}$ (kΩ)</th><th>Opto Series Resistor, $R_{FB1}$ (Ω)</th><th>Feedback Capacitor, $C_{FB1}$ (nF)</th><th>Series Diode $D_{FB}$ Required?</th></tr>
<tr><td>5</td><td>4.3</td><td rowspan="6">1</td><td rowspan="6">220</td><td rowspan="6">100</td><td rowspan="3">No</td></tr>
<tr><td>8</td><td>7.5</td></tr>
<tr><td>12</td><td>11</td></tr>
<tr><td>18</td><td>16</td><td rowspan="3">Yes</td></tr>
<tr><td>24</td><td>22</td></tr>
<tr><td>30</td><td>28</td></tr>
</table>

*Table 5. Zener Feedback Arrangement and Typical Component Values.*

Many capacitor manufacturers provide factors that increase the ripple current rating as the capacitor operating temperature is reduced from its data sheet maximum value. This should be considered in order to ensure that the capacitor is not oversized.

**ESR Specification**

The switching ripple voltage is equal to the peak secondary current multiplied by the ESR of the output capacitor. It is therefore important to select low ESR capacitors to reduce the ripple voltage. In general, selecting a high ripple current rated capacitor results in an acceptable value of ESR.

**Voltage Rating**

Select a voltage rating such that $V_{RATED} \geq 1.25\ V_O$.

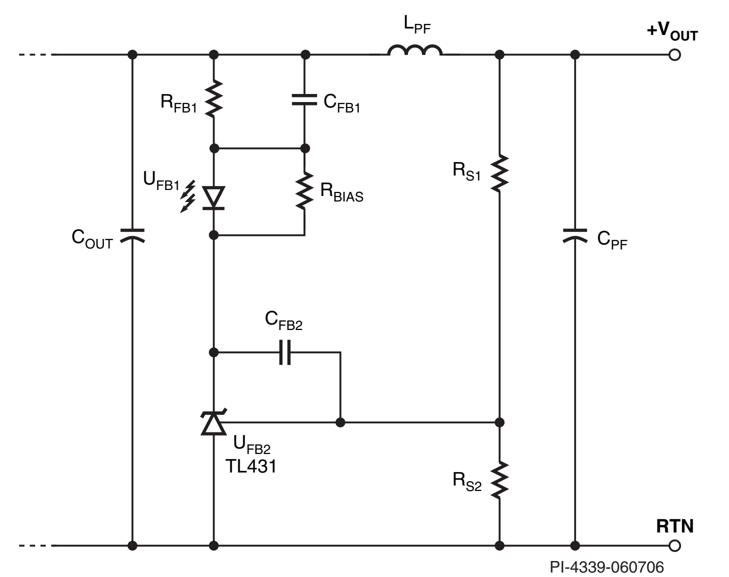
### Step 12 – Select Feedback Circuit Components

The feedback loop is arranged to draw the disable current (240 µA) from the EN/UV pin when the output voltage reaches regulation. Ideally, the feedback loop should be able to respond to the ripple on the output capacitor cycle-by-cycle.

Due to the high switching frequency, a high gain optocoupler of 300-600% is recommended to minimize feedback delay. Adding a capacitor across the DC gain setting resistor (R12 in Figure 1) further increases high frequency gain.

Table 5 shows a typical implementation of Zener feedback. The series drops across $D_{FB}$, $VR_{FB}$, $R_{FB1}$ and the forward drop of the LED $U_{FB1}$ determine the output voltage. Diode $D_{FB}$ is optional, depending on the availability of a suitable zener voltage. Resistor $R_{BIAS}$ provides a 1 mA bias current so that $VR_{FB}$ is operating close to its knee voltage. Resistor $R_{FB1}$ sets the DC gain of the feedback. Both resistors can be 0.125 W or 0.25 W, 5%. To increase high frequency gain, a ceramic capacitor $C_{FB1}$ is placed across $R_{FB}$. Selecting a Zener with a low test current (5 mA) will minimize the current needed to bias the feedback network, reducing no-load input power consumption.

Table 6 shows a typical implementation using a reference IC for improved accuracy. Reference $U_{FB2}$ is used to set the output voltage, programmed via the resistor divider $R_{S1}$ and $R_{S2}$. Resistor $R_{BIAS}$ provides the minimum operating current for $U_{FB2}$ while $R_{FB1}$ sets the DC gain. Capacitor $C_{FB2}$ rolls off the gain




| Output Voltage (V) | Feedback Bias Resistor, $R_{BIAS}$ (kΩ) | Opto Series Resistor, $R_{FB1}$ (Ω) | Feedback Capacitor, $C_{FB1}$ (nF) | Feedback Capacitor, $C_{FB2}$ (nF) | Series Resistor 1, $R_{S1}$ (kΩ) 1% | Sense Resistor 2, $R_{S1}$ (kΩ) 1% |
|---|---|---|---|---|---|---|
| 5 | 1 | 27 | 330 | 100 | 10 | 10 |
| 8 | | 91 | 150 | | 22.1 | |
| 12 | | 160 | 100 | | 38.3 | |
| 18 | | 430 | 100 | | 86.6 | |
| 24 | | 470 | 100 | | 102 | |
| 30 | | 510 | 47 | | 110 | |

*Table 6. Example of Reference IC Feedback Configuration.*

of $U_{FB2}$ so that it does not respond to the cycle-by-cycle output ripple voltage. AC feedback is provided directly through the optocoupler with $C_{FB1}$ increasing the gain.

If necessary, a post filter ($L_{PF}$ and $C_{PF}$) can be added to reduce high frequency switching noise and ripple. Inductor $L_{PF}$ should be in the range of 1 µH – 3.3 µH with a current rating above the peak output current. Capacitor $C_{PF}$ should be in the range of 100 µF to 330 µF with a voltage rating $\geq 1.25 \times V_{OUT}$. If a post filter is used, the optcoupler should be connected (as shown in Table 6) before the post filter inductor, and the sense resistors after the post filter inductor (when applicable).

## Design Tips

### Overcurrent and Overvoltage Protection Circuits

In some applications, it may be necessary to protect the load in fault conditions such as output overcurrent (OCP) or overvoltage (OVP). For example, if the load is a motor, then OCP can prevent the motor from overheating if it is stalled. Similarly, if the feedback loop is opened then the load can be protected from excessive voltage by overvoltage shutdown.

The smart AC sense feature of *PeakSwitch* simplifies implementation of such protection by providing the latching function on the primary side. Figure 15 shows a combined overcurrent and overvoltage shutdown circuit. The circuit is arranged so that if either overcurrent or overvoltage occurs, then SCR Q2 is turned on, shorting the output. Normally, this component would have to be sized to dissipate significant power. However, when the arrangement is used with *PeakSwitch,* the smart AC sense and latch-off feature will shut down the supply.

For OCP, resistor R1 senses the output current, turning on transistor Q1 when the voltage drop across R1 exceeds the $V_{BE}$ of Q1. Resistor R2 and C1 set a time constant allowing short term peak current but triggering the OCP in a true fault. Resistor R3 limits the current into the gate of Q2.

For OVP, Zener diode VR1 is selected such that it conducts when the output voltage exceeds the acceptable range, turning on Q2. Resistor R4 limits the Zener current and determines the turn-on point for Q2. Capacitor C2 provides decoupling, preventing false triggering of Q2 due to noise.

Transistor Q1 can be any small signal PNP bipolar transistor. The value of R1 is given by $V_{BE(Q1)} / I_{OCP}$, and power rating $V_{BE(Q1)} \times I_{OCP}$ where $I_{OCP}$ is the desired overcurrent trip point and $V_{BE(Q1)}$ is the base-emitter drop of Q1. The initial values of R2 and C1 are selected such that $3\tau \geq t_{TRIP}$ where $\tau = R2 \times C1$ and $t_{TRIP}$ is the minimum trip time in seconds. Use a starting value of 1 kΩ for R2, then optimize based on measured trip time, as peak to continuous current levels affect actual timing. Select R3 to exceed the worst case gate trigger current of Q2, when Q1 conducts. Values of 1 kΩ to 4.7 kΩ are typical. Select the Zener voltage of VR1 to be above the normal output voltage tolerance range, including the tolerance of VR1 itself. Resistor R4 is a 0.25 W, 100 Ω part and C2 is a small, 100 nF ceramic. SCR Q2 should be selected with a current rating above the continuous output current of the supply. For example for a 1 A output, a 2 A SCR would be a good choice. The anode of Q2 can be directly connected to the anode of the output diode, so that when fired, the secondary winding is shorted. This removes the need for the SCR to discharge the output capacitor and may allow a smaller current rating device to be selected. However, an additional ultra-fast diode must be placed in series with the SCR to block reverse current (see D10 in Figure 1).

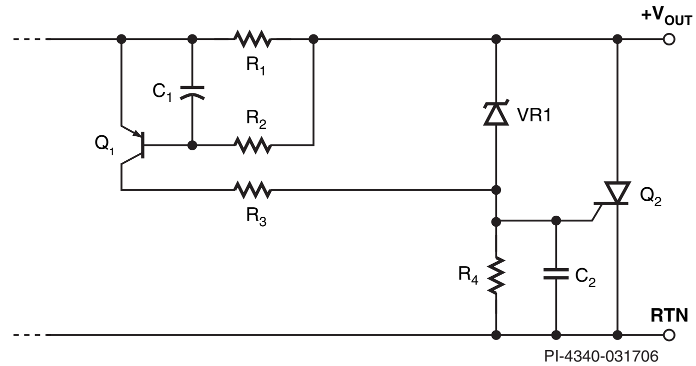



*Figure 15. Example of Combined Secondary Over Current and Overvoltage Protection Circuit.*

In designs where the latching feature is not used, a larger current rating SCR may be required.

### Transformer Core Sizing

The high switching frequency of *PeakSwitch* allows the selection of small core sizes that will adequately process the peak power. However, the small core size reduces the amount of winding window area available. This reduces the amount of copper for the windings, increasing winding losses.

In designs where the ratio of peak to continuous power is low (<~2), the transformer size may need to be increased to reduce losses and transformer heating. Acceptable temperature rise of the transformer should be verified at worst-case ambient temperature and maximum load.

### On-Time Extension

The on-time extension function of *PeakSwitch* maximizes the power delivered to the load when the DC input (bulk capacitor) voltage is low. This may allow the use of a smaller input capacitor in designs where the output can droop under peak load, especially in applications where the supply must pass line brown-out or missing AC cycle tests. On-time extension also increases the typical hold-up time.

Figure 16 is an example showing the effect of on-time extension during a line brownout event.

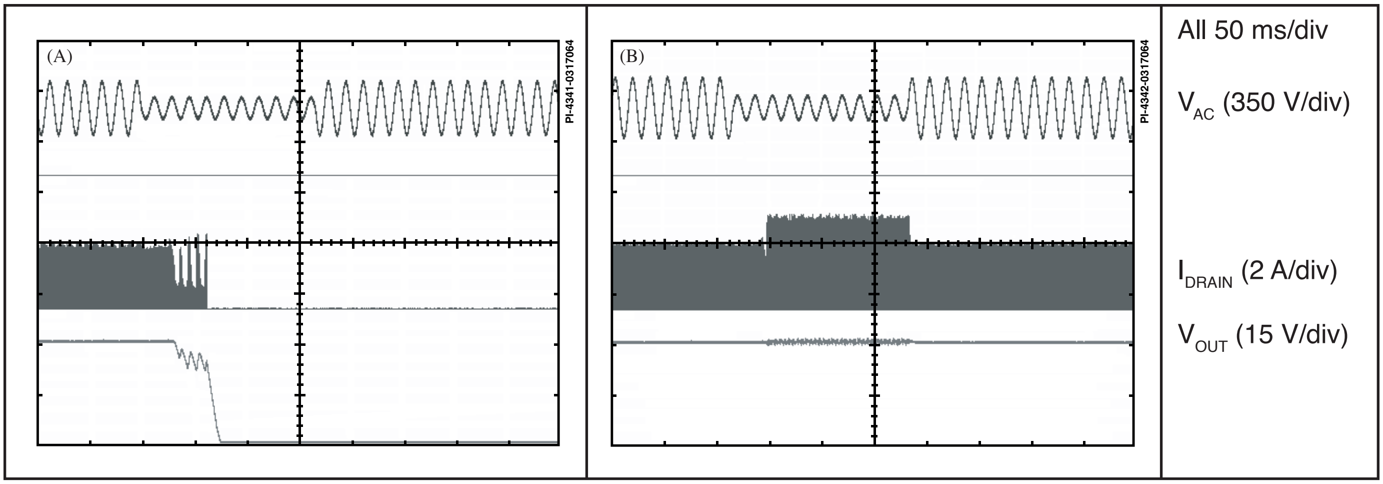



*Figure 16. Effect of On-Time Extension Operation During Line Brown-Out. (A) Without On-Time Extension Regulation is Lost. (B) With On-Time Regulation is Maintained.*

If the EN/UV pin has not been pulled low for 750 µs to 1.2 ms and every enabled switching cycle has terminated because DMAX was reached (instead of current limit), the on-time extension function is enabled. The maximum duty cycle limit is then disabled and switching cycles are terminated by current limit alone. Therefore, the MOSFET on time is only determined by the time for the primary current to reach current limit. The off time of the MOSFET remains fixed at $(1-D_{MAX}) \times 1/f_S$, where $D_{MAX}$ is the maximum duty cycle and $f_S$ the switching frequency. Once the EN/UV pin has been pulled low, indicating the output is again in regulation, on-time extension is disabled, and the MOSFET on time is terminated either by current limit or maximum duty cycle.

Since on-time extension is only enabled after the EN/UV pin has not been pulled low for up to 1.2 ms, the output may also have been out of regulation for that duration. Therefore, verify that the output voltage ripple is acceptable during instances of on-time extension.

## Other Information

**Adaptive Current Limit**

*PeakSwitch* incorporates an adaptive current limit function. When the current-limit state machine has the current limit set to 100% and an enabled switching cycle that follows a disabled switching cycle reaches current limit before DMAX, the adaptive current limit function reduces the current limit by about 10%. Once a cycle is skipped, the current limit is returned to the 100% value. This simplifies compliance with power limited source safety testing by limiting the overload power at high line.

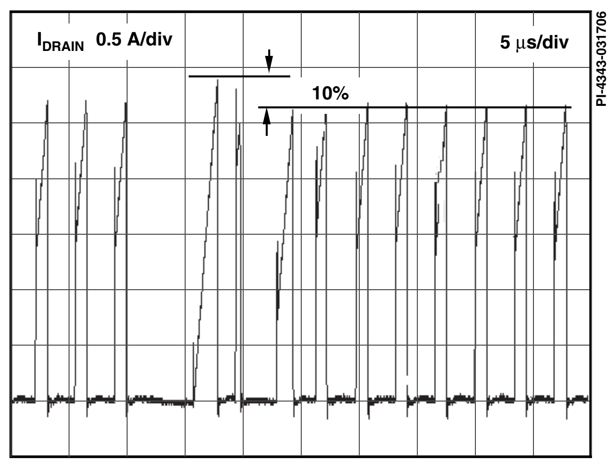



*Figure 17. Example of Adaptive Current Limit.*

## Layout Guidelines

See data sheet for layout guidelines.

## Quick Design Checklist

See data sheet for quick design checklist.

| Revision | Notes | Date |
|---|---|---|
| A | - | 3/06 |
| B | Corrected formatting and text errors. | 4/06 |
| C | Revised device symbol in Figure 1 to be consistent with other PI documentation (added second ground connection). | 5/06 |
| D | Revised grounding in Figure 1 to match actual implementation. | 6/06 |
| E | Added PKS607. | 2/07 |



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