



# SG320240B ( 320 DOTS X 240 DOTS )

## ■ FEATURES

- ◆ RECOMMENDED CONTROLLER
- ◆ (HD64646/MSM6225/SED1335)
- ◆ +5 V POWER SUPPLY
- ◆ 1/240 DUTY CYCLE
- ◆ EDGE LIGHTING TYPE CCFL BACKLIGHT

## ■ MECHANICAL DATA

| ITEM                    | DIMENSIONS           | UNIT |
|-------------------------|----------------------|------|
| Module Size (W x H x T) | 160.0 x 109.0 x 11.0 | mm   |
| Viewing Area (W x H)    | 122.0 x 92.0         | mm   |
| Active Area (W x H)     | 115.19 x 86.39       | mm   |
| Dot Size (W x H)        | 0.35 x 0.35          | mm   |
| Dot Pitch (W x H)       | 0.36 x 0.36          | mm   |

## ■ INTERFACE PIN CONNECTIONS

| NO. | SYMBOL          | LEVEL | FUNCTION                               |
|-----|-----------------|-------|----------------------------------------|
| 1   | DB0             | H/L   | Data Bit0                              |
| 2   | DB1             | H/L   | Data Bit1                              |
| 3   | DB2             | H/L   | Data Bit2                              |
| 4   | DB3             | H/L   | Data Bit3                              |
| 5   | /DISPOFF        | H/L   | Display OFF . Active LOW .             |
| 6   | FLM             | H     | Frame Start Signal                     |
| 7   | NC              | -     | No Connection .                        |
| 8   | CL1             | H→L   | Common Driver Data Shift Signal        |
| 9   | CL2             | H→L   | Clock Pulse For Segment Shift Register |
| 10  | V <sub>DD</sub> | 5V    | Power Supply Voltage                   |
| 11  | V <sub>SS</sub> | 0V    | Power Supply Ground                    |
| 12  | V <sub>EE</sub> | -     | Power Supply Voltage For LCD           |
| 13  | V <sub>O</sub>  | -     | Contrast Adjustment Voltage            |
| 14  | FGND            | -     | Frame Ground                           |

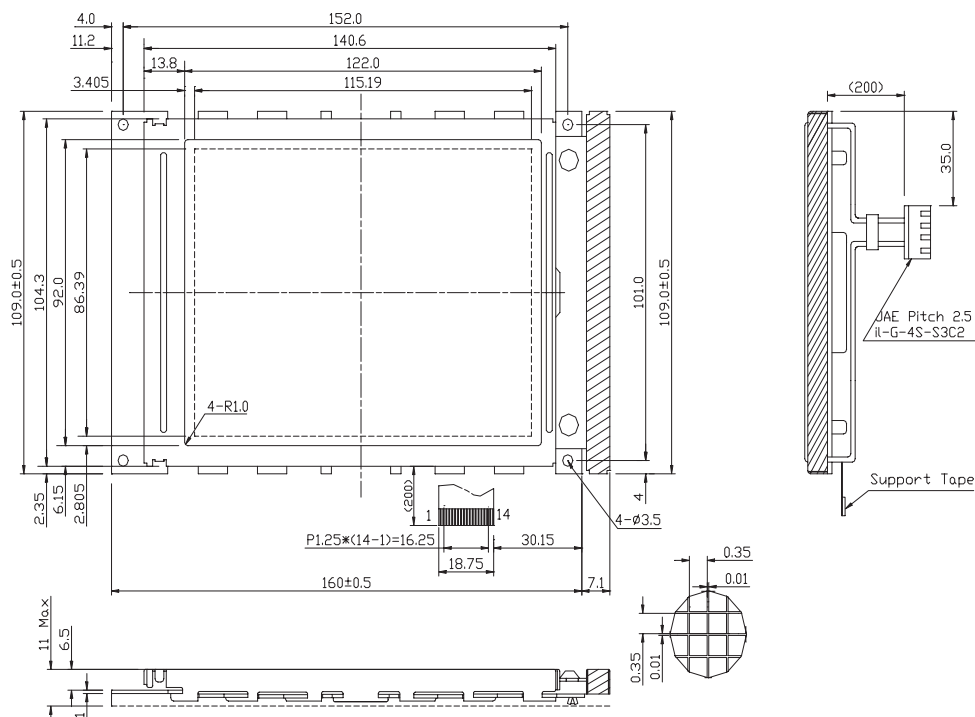
## ■ ABSOLUTE MAXIMUM RATINGS

| ITEM                         | SYMBOL                           | MIN.            | TYP. | MAX.            | UNIT |
|------------------------------|----------------------------------|-----------------|------|-----------------|------|
| Supply Voltage For Logic     | V <sub>DD</sub> -V <sub>SS</sub> | 0               | -    | 7               | V    |
| Supply Voltage For LCD Drive | V <sub>DD</sub> -V <sub>O</sub>  | 0               | -    | 30              | V    |
| Input Voltage                | V <sub>I</sub>                   | V <sub>SS</sub> | -    | V <sub>DD</sub> | V    |

## ■ ELECTRICAL CHARACTERISTICS

| ITEM                     | SYMBOL                           | CONDITION                   | MIN. | TYP. | MAX. | UNIT              |
|--------------------------|----------------------------------|-----------------------------|------|------|------|-------------------|
| Supply Voltage For Logic | V <sub>DD</sub> -V <sub>SS</sub> | -                           | 4.5  | 5    | 5.5  | V                 |
| LCD Supply Voltage       | V <sub>DD</sub> -V <sub>O</sub>  | V <sub>DD</sub> =5V Ta=25°C | 22.4 | 23.5 | 24.3 | V                 |
| Supply Current           | I <sub>DD</sub>                  | V <sub>DD</sub> =5V         | -    | 16   | 25   | mA                |
| Input Voltage            | "HIGH" Level                     | V <sub>IH</sub>             | -    | 2.2  | -    | V <sub>DD</sub> V |
|                          | "LOW" Level                      | V <sub>IL</sub>             | -    | -    | -    | 0.6 V             |
| Output Voltage           | "HIGH" Level                     | V <sub>OH</sub>             | -    | 2.4  | -    | V                 |
|                          | "LOW" Level                      | V <sub>OL</sub>             | -    | -    | -    | 0.4 V             |

## ■ EXTERNAL DIMENSIONS

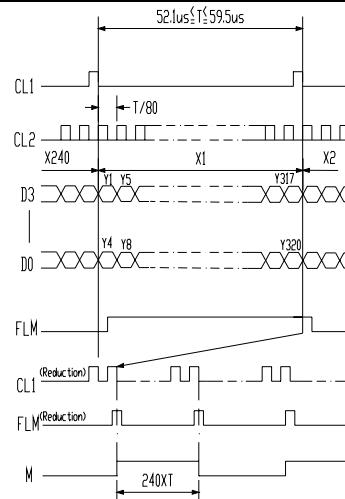
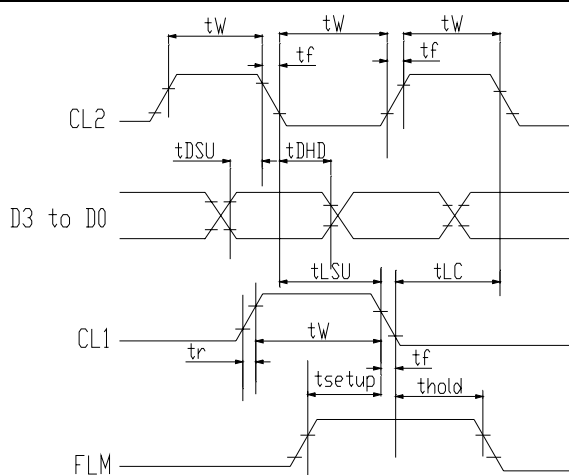




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## ■ TIMING CHARACTERISTICS

| ITEM                       | SYMBOL      | MIN. | TYP. | MAX. | UNIT. |
|----------------------------|-------------|------|------|------|-------|
| Frequency Of Maximum Clock | $f_{CP}$    | -    | -    | 8    | MHZ   |
| CL1 , CL2 , Pulse Width    | $t_w$       | 45   | -    | -    | ns    |
| Rise , Fall Time           | $t_r, t_f$  | -    | -    | 15   | ns    |
| Data Setup Time            | $t_{DSU}$   | 20   | -    | -    | ns    |
| Data Hold Time             | $t_{DHD}$   | 20   | -    | -    | ns    |
| CL1 Setup Time             | $t_{LSU}$   | 80   | -    | -    | ns    |
| CL1 → CL2 Time             | $t_{LC}$    | 80   | -    | -    | ns    |
| FLM Setup Time             | $t_{setup}$ | 100  | -    | -    | ns    |
| FLM Hold Time              | $t_{hold}$  | 100  | -    | -    | ns    |
| M Delay Time               | $t_{DF}$    | -    | -    | 300  | ns    |



## ■ BLOCK DIAGRAM

