Small signal combination IC for colour TV

TDA8302

FEATURES

- Gain controlled vision IF amplifier
- Synchronous demodulator for negative demodulation
- AGC detector operating on peak sync
- Tuner AGC
- AFC circuit with sample-and-hold and on/off-switch
- Video preamplifier
- Video switch to select either the internal video signal or an external video signal
- Horizontal synchronization circuit with two control loops
- Vertical synchronization (divider system), ramp generator for 60 Hz only
- Transmitter identification (mute)
- Sandcastle pulse generation
- VCR/auto VCR switch.

GENERAL DESCRIPTION

The device includes a three-stage video IF amplifier, AFC and AGC circuitry, integral three-level sandcastle pulse generator, fully synchronized horizontal and vertical time bases with drive circuits, a video switch and a transmitter identification/mute circuit. A functional colour TV receiver can thus be realised with the addition of a tuner, audio demodulator and amplifier, chrominance decoder and respective line and field deflection circuitry.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8302	32	DIL	plastic	SOT201

FUNCTIONAL DESCRIPTION

Video IF amplifier, demodulator and video amplifier

Each of the three AC-coupled IF stages permits the omission of DC feedback and possesses a control range in excess of 20 dB.

The IF amplifier is followed by a passive synchronous demodulator providing a regenerated carrier signal. This is limited by a logarithmic limiter circuit prior to its application to the demodulator. Improved picture synchronization is provided by a wider bandwidth together with improved video amplifier linearity. The video amplifier contains also a white spot inverter and a noise clamp which limits interference pulses to a point below the peak sync level.

AFC-circuit

The reference signal for the AFC quadrature demodulator can also be acquired from the tuned circuit of the IF synchronous demodulator because an accurate 90° phase shift is realised internally. In this way only one tuned circuit needs to be applied and only one adjustment has to be carried out. The AFC output is affected by the asymmetrical frequency spectrum of the signal fed to the quadrature demodulator, which is determined by the SAW filter characteristic. To overcome this video frequency dependency of the AFC output, the demodulator output is followed by a sample-and-hold circuit.
For the reception of negative-going signals, the output is sampled only during peak sync, where a non-modulated carrier is present. Substantial noise will be present on the quadrature demodulator input signal during reception of very weak signals. This noise has an asymmetrical frequency spectrum (with respect to the IF carrier) causing an offset in the AFC output voltage. This effect can be minimized by applying a notch in the demodulator tuned circuit. The sample-and-hold circuit is followed by an amplifier with high output impedance. The steepness of the of the AFC control voltage can be lowered by applying load resistors from the output to the supply and to ground. The AFC output is switched off when the AFC sample pin (22) is connected to ground.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage (pin 8)		10	12	13.2	V
I_P	supply current (pin 8)		90	115	140	mA
I_{start}	start current (pin 12)	note 1	-	6.5	9	mA
Video						
$V_{9\text{-}10(rms)}$	IF sensitivity (RMS value)	note 2	25	40	65	μV
$G_{9\text{-}10}$	IF gain control range		-	74	-	dB
S/N	signal-to-noise ratio	input signal = 10 mV	52	58	-	dB
V_{21}	AFC output voltage swing		10.5	-	11.5	V
Video switch						
$V_{16(p\text{-}p)}$	internal video input (peak-to-peak value)	V_O = 2.5 V(p-p)	-	2	-	V
$V_{13(p\text{-}p)}$	external video input (peak-to-peak value)	V_O = 2.5 V(p-p)	-	1	-	V
$V_{15(p\text{-}p)}$	video output signal (peak-to-peak value)		2.3	2.5	2.7	V
Sync						
V_{28}	required sync pulse amplitude	note 3	200	750	-	mV
I_{30}	required input current during flyback pulse		0.1	-	2	mA
V_{30}	sandcastle output during					
	burstkey		8	-	-	V
	horizontal blanking		4	4.4	5	V
	vertical blanking		2.1	2.5	2.9	V
V_{14}	video transmitter identification output					
	no signal condition		-	0.3	-	V
	signal condition		-	12	-	V
V_5	vertical feedback for DC voltage		2.9	3.3	3.7	V
$V_{5(p\text{-}p)}$	vertical feedback for AC voltage (peak-to-peak value)		-	1	-	V

Notes to the quick reference data

1. Supplying a current of 9 mA to pin 12 starts the horizontal oscillator. This current can be obtained via a bleed circuit from the mains rectifier whilst the main supply for the device (V_{cc}) is obtained from the horizontal output stage. The load current of the driver must be added to the value given.
2. On set AGC.
3. The minimum value is obtained by connecting a 1.8 kΩ resistor between pins 15 and 28. The slicing level can be varied by changing the value of this resistor (higher resistor value results in larger value of the minimum sync pulse amplitude). The slicing level is independent of the video information.

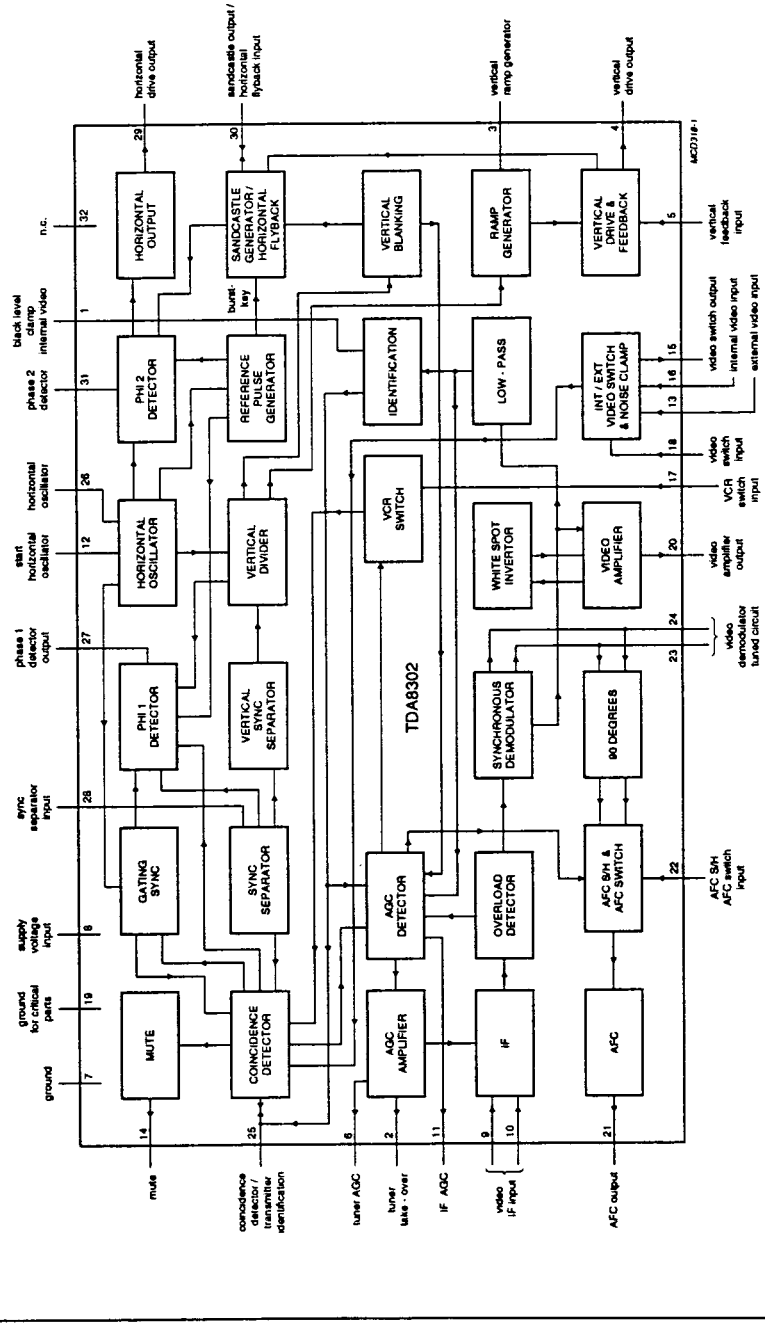


Fig.1 Block diagram.

PINNING

PIN	DESCRIPTION
1	black level clamp internal video
2	tuner take-over
3	vertical ramp generator
4	vertical drive
5	vertical feedback
6	tuner AGC
7	ground
8	supply voltage input
9	video IF input
10	video IF input
11	IF AGC
12	start horizontal oscillator
13	external video input
14	mute
15	video switch output
16	internal video input
17	VCR switch input
18	video switch input
19	ground for some critical parts
20	video amplifier output
21	AFC output
22	AFC S/H, AFC switch input
23	video demodulator tuned circuit
24	video demodulator tuned circuit
25	coincidence detector/transmitter identification
26	horizontal oscillator
27	phase 1 detector
28	sync separator input
29	horizontal drive output
30	sandcastle output/horizontal flyback input
31	phase 2 detector
32	not connected

The transmitter identification/coincidence detector

A mute signal (see Table 1) is generated to disable the audio preamplifier of an audio demodulator during the absence of a transmission signal. This prevents the emission of excessive noise from the loudspeaker, particularly when selecting an alternative program channel.

When the video switch is in the internal mode, the coincidence detector will be used as transmitter identification. Pin 25 is HIGH when the horizontal loop is synchronized with the video signal and LOW in the case of no-synchronization. In the external mode the IF part of the circuit has its own identification system. The system relies upon the detection of sync pulses on the incoming IF signal. The separated horizontal sync pulse charges the capacitor on pin 25 which drives the mute output (pin 14).

VCR switch

The TDA8302 has a separate pin (pin 17) for the VCR switch, see tables 2 and 4.

Due to the inherent instability of signals from a VCR, the horizontal time constant should be shorter to prevent loss of horizontal synchronization in the early part of the scan. Provision is therefore incorporated (in the auto VCR mode) to automatically switch the short time constant such that a strong signal instigates the 'VCR' mode and a weak signal triggers the 'TV' mode. The phase detector is gated during the 'TV mode' and operates with a slow time constant.

Video-switch

Video output from the device is filtered to remove the audio carrier and DC-coupled to pin 16. The TDA8302 provides the opportunity for a direct video connection (e.g. via a peritel connector) to be made to the device at pin 13. Selection between internal and external video is made by applying a switching potential to pin 18, see Table 3. The AGC detector is not gated during the external video mode, the first detector is also not gated and operates with a short time constant.

Table 1 MUTE truth Table

INPUT/OUTPUT	STATUS	STATUS	STATUS	STATUS	STATUS
Input signal Pins 9 and 10	60 Hz	none	60 Hz	60 Hz	none
output pin 25	9.5 V	0.3 V	9.5 V	9.5 V	0.3 V
input pin 28	60 Hz	none	60 Hz	none	60 Hz
input pin 18	LOW	LOW/ HIGH	HIGH	HIGH	HIGH
output pin 14	12 V	0.3 V	12 V	12 V	0.3 V

Table 2 VCR switch operation

INPUT	VCR MODE	AUTO VCR MODE	TV MODE
pin 17 (pin 18 = LOW)	HIGH	n.c.	LOW

Table 3 Video switch operation

INPUT	INTERNAL VIDEO	EXTERNAL VIDEO
pin 18	LOW	HIGH

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 8)	-	13.2	V
P_{tot}	total power dissipation	-	2.3	W
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	−25	+65	°C

QUALITY SPECIFICATION

Quality level according to UZW-BQ/FQ-601.

SYMBOL	PARAMETER	RANGE A	RANGE B	UNIT
ESD	protection circuit specification (note 1)	2000	500	V
		100	200	pF
		1500	0	Ω

Note to the Quality specification

1. All pins of the IC are protected against ESD by means of the internal clamping diodes. Range A represents the human body model and range B represents the charge device model.

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	30	35	K/W

Gain-reduction in the external video mode

The TDA8302 has an option to reduce the gain of the IF amplifier to prevent crosstalk from the IF to the horizontal oscillator when the circuit is in the external mode and there is no signal at the RF. The gain of the IF amplifier is reduced with 20 dB when the video-switch (see Table 3) is in the external video mode and pin 17 is connected with a resistor of 39 kΩ to ground. Without this resistor the IF remains at full gain. In the external video mode the 39 kΩ resistor has to be disconnected to achieve the auto VCR mode.

Horizontal synchronization

The horizontal synchronization circuit of the TDA8302 provides the drive pulse for a horizontal deflection stage.

- The phase of the control loop will be adapted automatically to the level of the input signal in order to achieve an optimum performance.
- The control gradient of the control loop will be low at reception of weak signals to reduce the noise bandwidth.
- The phase detector control current is increased during strong or no-signal reception to obtain a short catching time and a good performance during VCR playback.

Vertical synchronization

The TDA8302 embodies a synchronized divider system for generating the vertical sawtooth at pin 3 having several advantages and features such as:

- The advantage of the divider is that the vertical frequency is alignment free, and the provision of a maximum interference/disturbance protection.
- A discriminator-window checks the accuracy of the vertical trigger pulse.
- The divider system operates with a number of different reset windows. The windows are activated via an up/down counter. The counter increases its counter-value by 1 for each time the separated vertical sync pulse appears within the selected window, otherwise the counter value is lowered by 1.

Modes of operation

Large search window: divider ratio between 488 and 576.

This mode is valid for the following conditions:

- Divider is looking for a new transmitter
- Divider ratio found does not comply with the narrow window specification limits
- Up/down counter value of the divider system, operating in the narrow window mode, drops below count 10

Narrow window mode: divider ratio between 522 - 528 (60 Hz).

- The divider system switches over to narrow window mode when the up/down counter has reached his maximum value of 15 approved vertical sync pulses.
- When the divider operates in the narrow window mode and a vertical sync pulse is missing in the window, the divider is reset at the end of that window and the counter value is lowered by 1.
- At a counter value below 10 the divider system switches over to the large window mode.
- The divider system generate also the so-called anti-top-flutter pulse which inhibits the phase 1 detector during the vertical sync pulse. The width of this pulse depends on the divider mode. For the large window mode the start is generated at the reset of the divider. In the narrow window mode the anti-top-flutter pulse starts at the beginning of the first equalizing pulse. The anti-top-flutter pulse ends at count 12.
- The divider is switched to count 525 when out of sync is detected by the coincidence detector. This results in a stable amplitude when no input signal is available.

CHARACTERISTICS

T_{amb} = 25 °C;V_p = 12 V; carrier 38.9 MHz negative modulation, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 8)						
V_8	supply voltage range		10	12	13.2	V
I_8	supply current	no input	90	115	140	mA
I_{12}	start current (pin 12)	note 1	-	6.5	9	mA
V_{12}	start protection level	I_{12} = 12 mA	-	-	16.5	V
IF Amplifier						
$V_{9-10(rms)}$	input sensitivity (RMS value)	note 2	25	40	65	µV
R_{9-10}	differential input resistance	note 3	-	1300	-	Ω
C_{9-10}	differential input capacitance	note 3	-	5	-	pF
G_{9-10}	gain control range		-	74	-	dB
ΔV_{20}	output signal expansion for 46 dB input signal variation	note 4	-	1	-	dB
V_{9-10}	maximum input signal		100	170	-	mV
Video Amplifier (notes 5 and 6)						
V_{20}	zero signal output level		4.7	4.9	5.1	V
V_{20}	peak sync level		2.5	2.7	2.9	V
V_{20}	white spot threshold level		-	5.5	-	V
V_{20}	white spot insertion level		-	4	-	V
Z_{20}	video output impedance		-	25	-	Ω
I_{20}	internal bias current of npn emitter follower output transistor		1.4	1.8	-	mA
I_{source}	maximum source current (pin 20)		10	-	-	mA
B	bandwidth of demodulated output signal		5	6	-	MHz
G_{20}	differential gain	note 7	-	2	5	%
φ	differential phase	note 7	-	2	5	°
NL	video non linearity	note 8	-	2	5	%
	intermodulation 1.1 MHz; blue 1.1 MHz; yellow 3.3 MHz; blue 3.3 MHz; yellow	note 9	 50 50 55 55	 60 60 65 65	 - - - -	 dB dB dB dB
S/N	signal-to-noise ratio	10 mV input signal	52	58	-	dB
		end of gain control range; note 10; see Fig.5	57	62	-	dB
V_{20}	residual carrier signal		-	2	10	mV
V_{20}	residual 2nd harmonic of carrier signal		-	2	10	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF sync separator						
I_I	input current		0.4	0.6	0.8	mA
I_O	output current (pin 1)		22	27	32	µA
V_1	clamp level		-	3.3	-	V
Tuner AGC						
$V_{9\text{-}10(rms)}$	minimum starting point for tuner take-over (RMS value)		-	-	0.2	mV
$V_{9\text{-}10(rms)}$	maximum starting point for tuner take-over (RMS value)		100	150	-	mV
I_6	maximum tuner AGC output swing	V_6 = 3 V	4	-	-	mA
V_6	output saturation voltage	I_6 = 2 mA	-	-	300	mV
I_6	leakage current		-	-	1	µA
	input signal variation complete tuner control	ΔI_6 = 2 mA	0.2	2	4	dB
V_2	minimum voltage tuner take-over		-	-	1	V
Video Switching Circuit (note 12)						
EXTERNAL POSITIVE VIDEO INPUT						
$V_{13(p\text{-}p)}$	input signal (peak-to-peak value)	V_O = 2.5 V(p-p)	-	1	-	V
I_{13}	input current		-	1.5	5	µA
V_{13}	peak sync clamping level	I_{13} = 1 mA	1.65	1.85	2.05	V
INTERNAL VIDEO INPUT						
$V_{16(p\text{-}p)}$	Internal video input signal (peak-to-peak value	V_O = 2.5 V(p-p)	-	2	-	V
I_{16}	input current		-	1.5	5	µA
V_{16}	noise clamping level	I_{16} = 1 mA	2.2	2.4	2.6	V
POSITIVE VIDEO OUTPUT						
$V_{15(p\text{-}p)}$	video output signal (peak-to-peak value)		2.3	2.5	2.7	V
V_{15}	peak sync signal		-	3	-	V
I_{bias}	internal bias current (pin 15)		1	1.5	-	mA
I_O	maximum output current (pin 15)		5	-	-	mA
α	crosstalk external to internal	notes 12 and 13	-	55	-	dB
α	crosstalk internal to external	notes 12 and 13	-	55	-	dB
Video switch						
V_{18}	input voltage for internal video		-	-	0.8	V
V_{18}	input voltage for external video		2	-	V_P	V
I_{18}	maximum current	V_{18} = 0 V	-	0.05	0.2	mA
		V_{18} = 12 V	-	0.25	1	mA
AFC-circuit (note 14)						
I_{22}	AFC sample and hold switch-off current		0.1	-	-	mA
I_O	output current (pin 22)	V_{22} = 0 V	0.2	0.4	0.8	mA
I_{IL}	leakage current (pin 22)		-	-	1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{21}	AFC output voltage swing		10.5	-	11.5	V
I_{21}	available output current		±0.2	-	-	mA
	control slope		-	100	-	mV/kHz
V_O	output voltage (pin 21)	AFC off	5.5	6	6.5	V
R_O	AFC output resistance		-	40	-	kΩ
$V_{21(p-p)}$	output voltage swing	notes 11 and 15	-	11	-	V
	control slope	notes 11 and 15	-	80	-	mV/kHz
V_{21}	output voltage shift with respect to V_I = 10 mV(RMS)	notes 11 and 15	-	−2	-	V
Sync separator (see Fig.6)						
V_{28}	required sync pulse amplitude	note 16	200	750	-	mV
I_{28}	input current	V_{28} > 5 V	-	8	-	µA
		V_{28} = 0 V	-	−10	-	mA
First control loop						
Δf	PLL holding range		-	±1500	±2000	Hz
Δf	PLL catching range		±600	±1500	-	Hz
	control sensitivity to oscillator	note 17	see Fig.7			
Second control loop (positive edge)						
$\frac{\delta t_d}{\delta t_o}$	control sensitivity, see Fig.6	note 18	-	100	-	
t_d	control range		-	25	-	µs
Phase adjustment (via second control loop)						
	control sensitivity		-	25	-	µA/µs
α	maximum allowed phase shift		-	±2	-	µs
Horizontal oscillator						
	free running frequency	R = 34.3 kΩ; C = 2.7 nF	-	15750	-	Hz
Δf	spread with fixed external components		-	-	4	%
Δf	frequency variations with supply voltage from 9.5 to 13.2 V		-	-	2	%
Δf_T	frequency variation with temperature	note 11	-	−1.6	-	Hz/°C
Δf_{lr}	maximum frequency deviation at start of horizontal output		-	-	10	%
Δf	frequency variation when only noise is received	note 11	-	-	500	Hz
Horizontal output (pin 29; open collector)						
V_{29}	output limiting voltage		-	-	16.5	V
V_{OL}	output voltage LOW	I_{sink} = 10 mA	-	0.3	0.5	V
I_{sink}	maximum sink current		10	-	-	mA
	duty factor of output signal		-	46	-	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	rise time output pulse		-	260	-	ns
t_f	fall time output pulse		-	100	-	ns
Flyback input and sandcastle output (note 19)						
I_{30}	required input current during flyback pulse		0.1	-	2	mA
V_{30}	output voltage during burstkey horizontal blanking vertical blanking		 8 4 2.1	 - 4.4 2.5	 - 5 2.9	 V V V
t_W	burstkey pulse width		2.9	3.3	3.7	µs
VERTICAL BLANKING						
	divider in search window		-	17	-	lines
	divider in narrow window		-	21	-	lines
t_d	delay between the start of the sync pulse at the video output and the burstkey pulse trailing edge rising edge		 - 4.7	 - 5.4	 9.4 6.1	 µs µs
VCR switch (non-VCR mode; V_{17} < 5 V)						
R_{17}	resistance to ground		-	-	5	kΩ
I_{17}	output current	pin 17 = 0 V	-	-	0.5	mA
VCR switch (auto-VCR mode)						
I_{source}	source current (pin 17)		-	-	30	µA
I_{sink}	sink current (pin 17)		-	-	30	µA
$V_{9-10(rms)}$	IF input signal for switching from fast to slow in auto VCR mode (RMS value)	pin 17 = n.c.	-	2.2	-	mV
VCR switch (VCR mode; V_{17} > 7 V)						
R_{17}	resistance to V_{CC}		-	-	5	kΩ
I_{17}	input current	$V_{17} = V_{CC}$	-	-	1	mA
Vertical ramp generator (note 20)						
I_3	input current during scan		-	-	2	µA
I_3	discharge current during retrace		-	0.8	-	mA
$V_{3(p-p)}$	sawtooth amplitude (peak-to-peak value)		-	1.9	-	V
t	interlace timing of the internal pulses	note 11	30	32	34	µs
Vertical output						
I_4	available output current	V_4 = 4 V	-	-	3	mA
V_4	maximum available output voltage	I_4 = 0.1 mA	4.4	5	-	V
Vertical feedback input						
V_5	DC input voltage		2.9	3.3	3.7	V
$V_{5(p-p)}$	AC input voltage (peak-to-peak value)		-	1	-	V
I_5	input current		-	-	12	µA
	internal pre-correction to sawtooth		-	3	-	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	temperature dependency of the amplitude	note 11 ΔT = 45 °C	-	-	2	%
Vertical guard						
ΔV_5	active switch level at a deviation with respect to the DC feedback level guard level LOW guard level HIGH	note 21	 - -	 1.5 2	 - -	 V V
Coincidence detector/transmitter identification (note 22)						
V_{25}	voltage for in-sync condition		-	9.8	-	V
V_{25}	voltage for no-sync condition	no signal	-	0.3	-	V
V_{25}	switching level to the phase detector from fast to slow		6.2	6.7	7.2	V
V_{25}	hysteresis slow to fast		-	0.6	-	V
V_{25}	switching level to activate the mute function (transmitter identification)		2.5	2.8	3.1	V
V_{25}	hysteresis mute function		-	2	-	V
Video transmitter identification output (open collector)						
V_{14}	output voltage active	no sync; I = 1 mA	-	0.3	0.5	V
I_{14}	sink current active		-	-	5	mA
I_{14}	output current inactive (transmitter present)		-	-	1	µA

Notes to the characteristics

1. Supplying a current of 9 mA to pin 12 starts the horizontal oscillator. This current can be obtained via a bleed circuit from the mains rectifier whilst the main supply for the device (V_{cc}) is obtained from the horizontal output stage. The load current of the driver must be added to the value given.
2. On set AGC.
3. The input impedance has been chosen such that a SAW filter can be employed.
4. Measured with 0 dB = 450 µV.
5. Measured at 10 mV RMS 100% input signal.
6. Projected zero point; i.e. with switched demodulator.
7. Measured according to the test line given in Fig.3. The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level. The differential phase is defined as the difference in degrees between the largest and smallest phase angle. The differential gain and phase are measured with a DSB signal.
8. This figure is valid for the complete video signal amplitude (peak white to black). The non-linearity is expressed as a percentage of the maximum deviation of a luminance step from the mean step, with respect to the mean step.
9. The test set-up and input conditions are given in Fig.5. The figures are measured at an input signal of 10 mV RMS.
10. Measured with a source impedance of 75 Ω.

$$\textit{The signal-to-noise ratio} = 20 \log \frac{V_o \ \textit{black-to-white}}{V_{n(rms)} \ \textit{at } B = 5 \ \textit{MHz}}$$

11. These figures are based on test samples.
12. When the video switch is in the external mode the first control loop in the synchronization circuit is not switched to a long time constant when weak signals are received.
13. Defined as $20 \log \frac{V_o \text{ unwanted video black-to-white}}{V_o \text{ wanted video-black-to-white}}$; measured at 4.4 MHz.
14. The indicated figures are measured at an input signal of 10 mV RMS. The unloaded Q-factor of the reference tuned circuit is 70. With very weak input signals the drive signal for the AFC circuit will have a high noise content. This noise input has a asymmetrical frequency spectrum which will cause an offset of the AFC output voltage. To avoid problems due to this effect a notch filter can be built into the demodulator tuned circuit. The characteristics given for weak signals are measured without a notch circuit, with a SAW filter connected in front of the IC input signal such that the input signal of the IC is 150 μV (RMS value).
15. Measured at an input signal amplitude of 150 μV(RMS) (pin 21).
16. The minimum value is obtained by connecting a 1.8 kΩ resistor between pins 15 and 28. The slicing level can be varied by changing the value of this resistor (higher resistor value results in larger value of the minimum sync pulse amplitude). The slicing level is independent of the video information.
17. Frequency control is obtained by supplying a correction current to the oscillator RC network via a resistor connected between the phase 1 detector output and the oscillator network. The oscillator can be adjusted to the correct frequency by short circuiting the sync separator bias network (pin 28) to $+V_p$. To avoid the need of a VCR switch the time constant of the phase detector at strong input signals is sufficiently short to get a stable picture during VCR playback. During the vertical retrace period the time constant is even shorter so that the head-errors of the VCR are compensated at the beginning of scan. During conditions of weak signal (information derived from the AGC circuit) the time constant is increased to obtain a better noise immunity.
18. This figure is valid for an external load impedance of 82 kΩ from pin 31 to the phase adjustment potentiometer (of H-shift).
19. The flyback input and sandcastle output have been combined on one pin. The flyback pulse is clamped to a level of 4.5 V. The minimum current to drive the second control loop is 0.1 mA.
20. The vertical scan is synchronized by means of a divider system. Therefore no frequency adjustment is required for the V-ramp generator.
21. To avoid screen burn due to a collapse of the vertical deflection a continuous blanking level (V_{30} = 2.5 V) is inserted in the sandcastle pulse when the feedback voltage of the vertical deflection is not within the specified limits.
22. The functions in-sync/out-of-sync and transmitter identification have been combined on this pin. The capacitor is charged during the sync pulse and discharged during the time difference between gating (6.5 μs) and the sync pulse in the internal video mode. When the circuit is in the external mode the capacitor is charged by the horizontal sync pulse and discharged continuously with a small current.

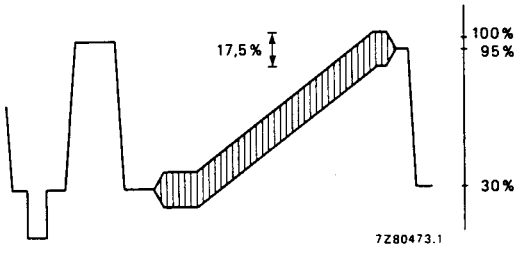


Fig.2 Video output signal.

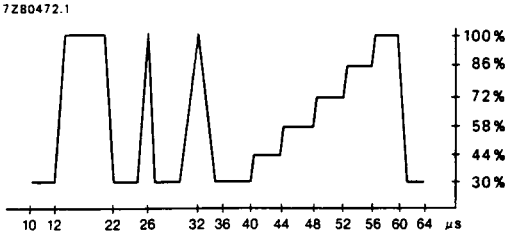
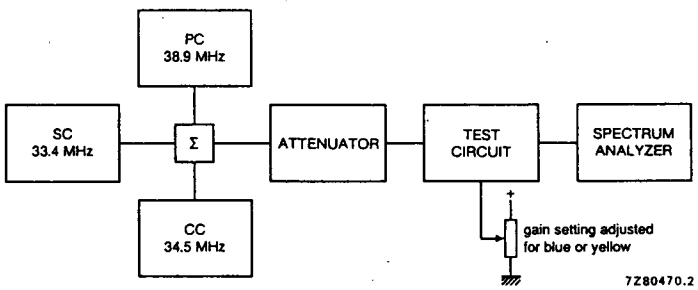
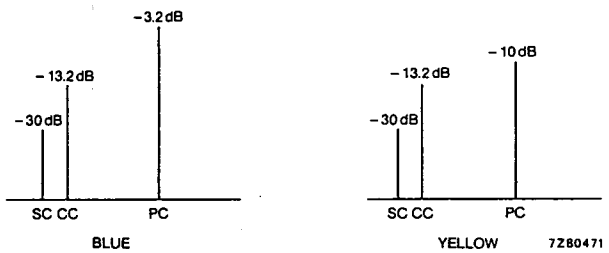


Fig.3 EBU test signal waveform (line 17).





Input signal conditions

SC = Sound carrier

CC = Chrominance carrier

PC = Picture carrier

All with respect to peak sync level

$$Value\ at\ 1.1MHz : 20 \log \frac{V_o\ at\ 4.4MHz}{V_o\ at\ 1.1MHz} + 3.6dB$$

$$Value\ at\ 3.3MHz : 20 \log \frac{V_o\ at\ 4.4MHz}{V_o\ at\ 3.3MHz}$$

Fig.4 Test set-up intermodulation.

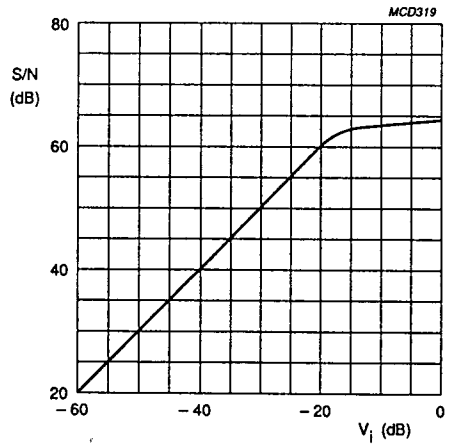
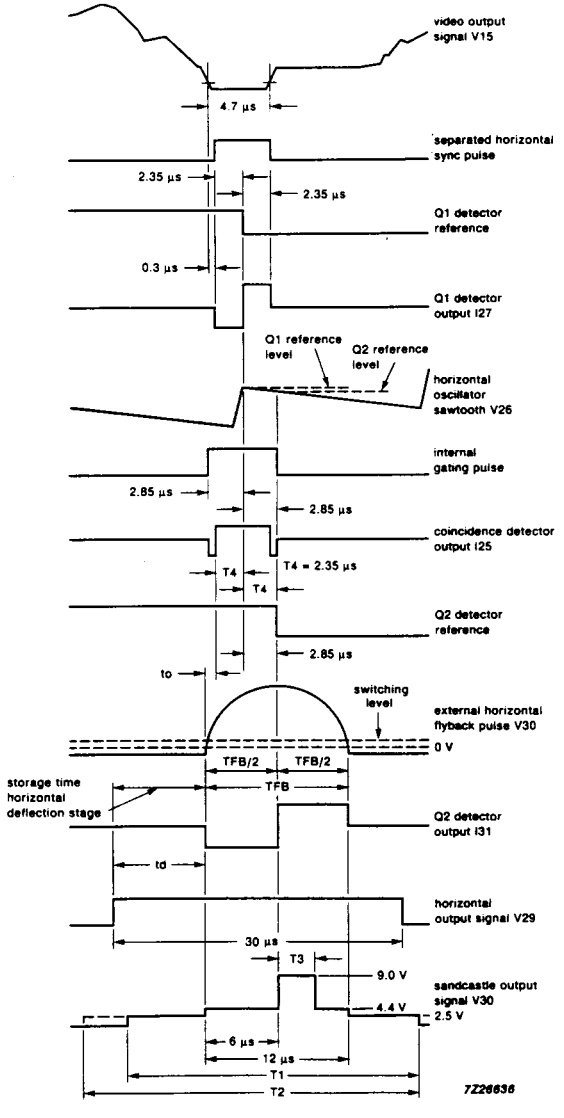


Fig.5 Signal-to noise ratio as a function of the input voltage (0 dB = 100 mV).



T1: divider in search window: 34p; $p = 1/2f_H$

T2: divider in narrow window: 42p

T3: 3.3 µs

Fig.6 Timing diagram.

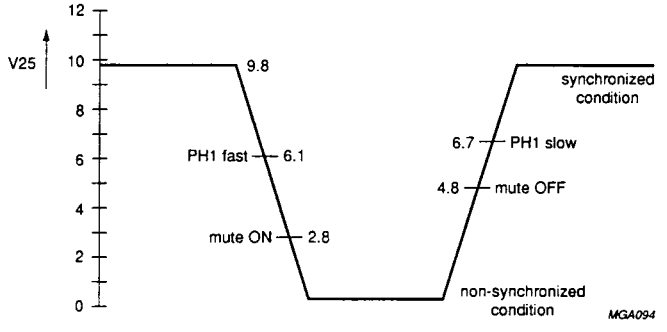


Fig.7 Switching levels coincidence detector.

Table 4

CONDITION PIN 18 VIDEO SWITCH	CONDITION PIN 17 VCR SWITCH	CONDITION V_{25}	CONTROL SENSITIVITY HOR.OSCILLATOR kHz / µs	
			T2 - T1	T3 = SCAN
Low internal video	floating automatic VCR	V_{25} > 6.7 V and strong signal	11.3	7.6
		V_{25} > 6.7 V and weak signal	1.3	1.3
		V_{25} < 6.1 V and strong signal	11.3	7.6
		V_{25} < 6.1 V and weak signal	11.3	7.6
	HIGH forced VCR	don't care	11.3	7.6
	LOW T.V. mode	V_{25} > 6.7 V	1.3	1.3
		V_{25} < 6.1 V	11.3	7.6
HIGH or floating external video	don't care	don't care	11.3	7.6

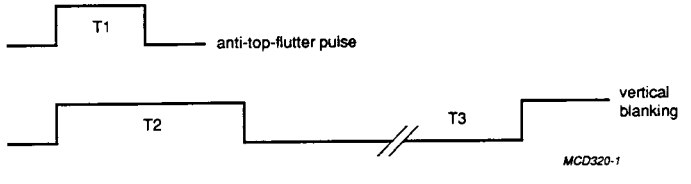


Fig.8 Anti-top-flutter pulse.

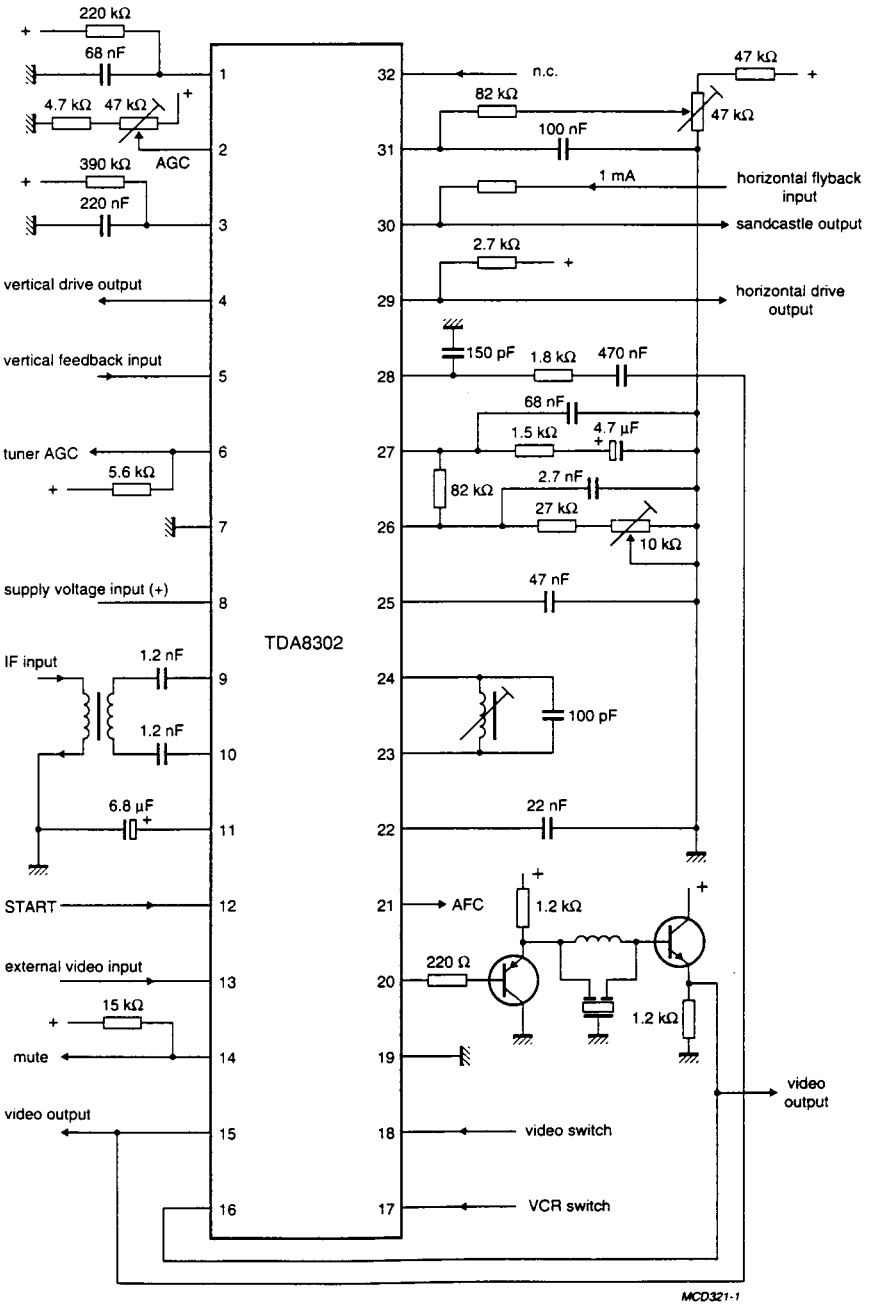


Fig.9 Application diagram.