LNK33x2-7D
LinkSwitch-TNZ Family

Energy Efficient Off-line Switcher IC with Best-in-Class
Light Load Efficiency and Lossless AC Zero-Cross Detection

Product Highlights

Highest Performance and Design Flexibility

- Lossless zero cross signal generation
- Supports buck, buck-boost and flyback topologies
- Enables ±3% regulation across line and load
- Selectable device current limit
- 66 kHz operation with accurate current limit
  - Allows the use of low-cost off-the-shelf inductors
  - Reduces size and cost of magnetics and output capacitor
- Frequency jittering reduces EMI filter complexity
- X capacitor discharge function (LNK331x only)

Enhanced Safety and Reliability Features

- Soft-start limits system component stress at start-up
- Auto-restart for short-circuit and open loop faults
- Output overvoltage protection (OVP)
- Line input overvoltage protection (OVL)
- Hysteretic over-temperature protection (OTP)
- Extended creepage between DRAIN pin and all other pins improves field reliability
- 725 V MOSFET rating for excellent surge withstand
- Nemko (EN62368-1) and CB (IEC62368-1) certifications

EcoSmart™– Extremely Energy Efficient

- IC standby supply current <100 μA
- On/Off control provides constant efficiency over a wide load range
- Easily meets all global energy efficiency regulations
- No-load consumption <30 mW with external bias

Applications

- Home and building automation
- Dimmers, switches and sensors with and w/o Neutral wire
- Appliances
- IoT and industrial controls

Description

The LinkSwitch™-TNZ family of ICs combine power conversion with lossless generation of AC zero crossing signal used typically for system clock and timing functions. Designs using the highly integrated LinkSwitch-TNZ ICs are more flexible than discrete implementations reducing component count by 40% or higher. Besides enabling 80+ efficiencies in low power flyback designs, very low consumption at light loads enabled by On/Off control allow for more functions (display, wireless connectivity, sensors etc.) to be active during system standby. The device family supports buck, buck-boost and flyback converter topologies.

Each device incorporates a 725 V power MOSFET, oscillator, a high-voltage switched current source for self-biasing, frequency jittering, fast (cycle-by-cycle) current limit, hysteretic thermal shutdown, and output and input overvoltage protection circuitry onto a monolithic IC.

LinkSwitch-TNZ ICs consume <100 μA current in standby resulting in power supply designs that can meet no-load and standby regulations worldwide. MOSFET current limit modes can be selected through the BYPASS pin capacitor value. The high current limit level provides maximum continuous output current while the low level permits using very low-cost and small surface mount inductors. A full suite of protection features enables safe and reliable power supplies protecting the device and the system against input and output overvoltage faults, device over-temperature faults, lost regulation, and power supply output overload or short-circuit faults.

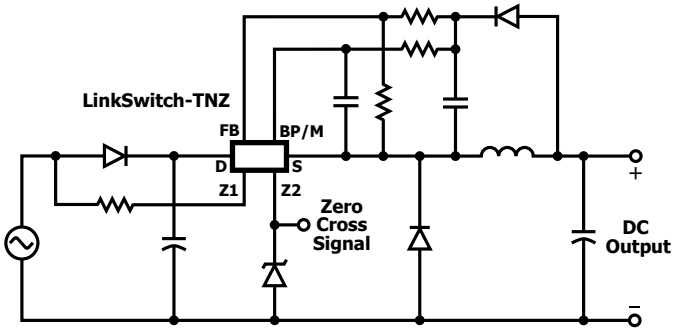


Figure 1. Typical Buck Converter Application (See Application Examples Section for Flyback and other Circuit Configurations).

Figure 2. Package D: SO-8C.

Output Current in Buck Table[1]

Product	230 VAC ± 15%		85-265 VAC	
	MDCM[2]	CCM[3]	MDCM[2]	CCM[3]
LNK33x2D	63 mA	80 mA	63 mA	80 mA
LNK33x4D	120 mA	170 mA	120 mA	170 mA
LNK33x6D	225 mA	360 mA	225 mA	360 mA
LNK33x7D	360 mA	575 mA	360 mA	575 mA

Table 1. Output Power Table.
Notes:
1. Typical output current in a non-isolated buck converter with devices operating at default current limit and adequate heat sinking. Output power capability depends on respective output voltage and thermal requirements. See Key Applications Considerations section for complete description of assumptions, including fully discontinuous conduction mode (DCM) operation.
2. Mostly discontinuous conduction mode.
3. Continuous conduction mode.

Output Power in Flyback Table[6]

Product	Open Frame[4]	
	230 VAC ± 15%	85-265 VAC
LNK33x2D	5 W	3 W
LNK33x4D	10 W	6 W
LNK33x6/7D[5]	18 W	12 W

Table 2. Output Power Table.
Notes:
4. Maximum practical continuous power in an open frame design with adequate heat sinking, measured at 25 °C ambient.
5. LNK33x6 is recommended in Flyback for highest efficiency.
6. See Key Application Considerations section for complete description of assumptions.

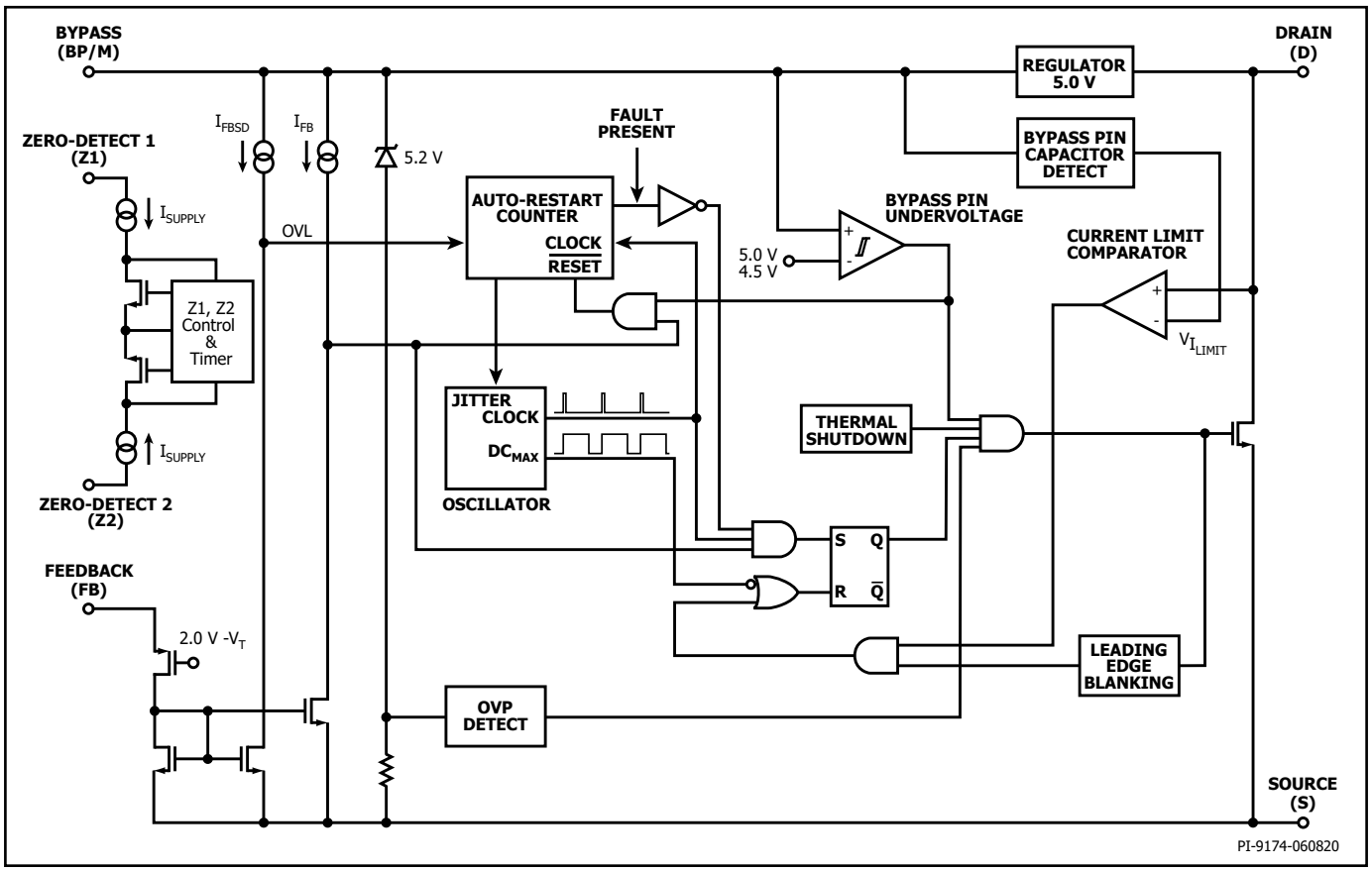


Figure 3. Functional Block Diagram.

Pin Functional Description

Z1 and Z2 Pins

- Z1 and Z2 are used in combination for zero cross detect (ZCD) signal generation, X capacitor discharge or both.
- For zero crossing, Z1 is connected to one of the input AC lines through an external resistor while Z2 forms the ZCD signal output.
- For X capacitor discharge (LNK331x only), Z1 is connected to one AC line input through an external resistor and Z2 is connected to the other AC input line input through a separate external resistor.
- Z1 and Z2 can also be used to combine X capacitor discharge and ZCD signal generation functions (LNK331x only) – see Application Section for details.
- Z1 and Z2 can be connected to SOURCE (S) pins if not used.
- Z1 and Z2 are interchangeable.

DRAIN (D) Pin

Power MOSFET drain connection. Provides internal operating current for both start-up and steady-state operation.

BYPASS (BP/M) Pin

This pin has multiple functions:

- It is the connection point for an external bypass capacitor for the internally generated 5.0 V supply.
- It is a mode selector for the current limit value, depending on the value of the capacitance added. Use of a 0.1 µF capacitor results in the standard current limit value. Use of a 1 µF capacitor results in the current limit being reduced, allowing design with lowest cost surface mount buck chokes.
- It provides a shutdown function. When the current into the BYPASS pin exceeds I_{BPSD} for a time equal to 2 to 3 cycles of the internal oscillator (f_{OSC}), the device enters auto-restart. This can be used to provide an output overvoltage protection function with external circuitry.

FEEDBACK (FB) Pin

During normal operation, switching of the power MOSFET is controlled by the FEEDBACK pin. MOSFET switching is terminated when a current greater than I_{FB} (49 µA) is delivered into this pin. Line overvoltage protection is detected when a current greater than I_{FBSD} (670 µA) is delivered into this pin for 2 consecutive switching cycles.

SOURCE (S) Pin

This pin is the power MOSFET source connection. It is also the ground reference for the BYPASS and FEEDBACK pins.

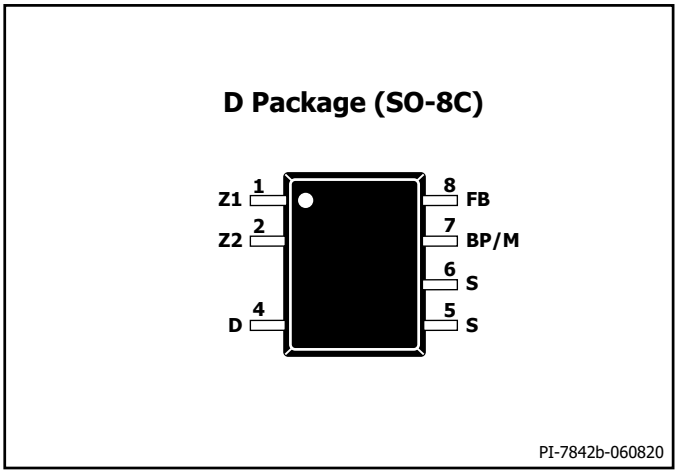


Figure 4. Pin Configuration.

LinkSwitch-TNZ Functional Description

LinkSwitch-TNZ combines a high-voltage power MOSFET switch with a power supply controller in one device. Unlike conventional PWM (pulse width modulator) controllers, LinkSwitch-TNZ uses a simple ON/OFF control to regulate the output voltage. The LinkSwitch-TNZ controller consists of an oscillator, feedback (sense and logic) circuit, 5.0 V regulator, BYPASS pin undervoltage circuit, over-temperature protection, line and output overvoltage protection, frequency jittering, current limit circuit, leading edge blanking and a 725 V power MOSFET. The LinkSwitch-TNZ incorporates additional circuitry for auto-restart.

Oscillator

The typical oscillator frequency is internally set to an average of f_{OSC} (66 kHz). Two signals are generated from the oscillator: the maximum duty cycle signal ($DC_{(MAX)}$) and the clock signal that indicates the beginning of each cycle.

The LinkSwitch-TNZ oscillator incorporates circuitry that introduces a small amount of frequency jitter, typically 4 kHz peak-to-peak, to minimize EMI emission. The modulation rate of the frequency jitter is set to 1 kHz to optimize EMI reduction for both average and quasi-peak emissions. The frequency jitter should be measured with the oscilloscope triggered at the falling edge of the DRAIN waveform. The waveform in Figure 5 illustrates the frequency jitter of the LinkSwitch-TNZ.

Soft-Start

At power-up or during a restart attempt in auto-restart, the device applies a soft-start by temporarily reducing the oscillator frequency to $f_{OSC(SS)}$ (typically 33 kHz). Soft-start terminates either after 256 switching cycles or if the output voltage reaches regulation.

Feedback Input Circuit

The feedback input circuit at the FEEDBACK pin consists of a low impedance source follower output set at V_{FB} (2.0 V). When the current delivered into this pin exceeds I_{FB} (49 µA), a low logic level (disable) is generated at the output of the feedback circuit. This output is sampled at the beginning of each cycle on the rising edge of the clock signal. If high, the power MOSFET is turned on for that cycle (enabled), otherwise the power MOSFET remains off (disabled). The sampling is done only at the beginning of each cycle. Subsequent changes in the FEEDBACK pin voltage or current during the remainder of the cycle do not impact the MOSFET enable/disable status. If a current greater than I_{FBSD} is injected into the FEEDBACK pin while the MOSFET is enabled for at least two consecutive cycles the part will stop switching and enter auto-restart off-time. Normal switching resumes after the auto-restart off-time expires. This shutdown function allows implementing line overvoltage protection in flyback converters (see Figure 6). The current into the FEEDBACK pin should be limited to less than 1.2 mA.

5.0 V Regulator and 5.2 V Shunt Voltage Clamp

The 5.0 V regulator charges the bypass capacitor connected to the BYPASS pin to V_{BP} by drawing a current from the voltage on the DRAIN, whenever the MOSFET is off. The BYPASS pin is the internal supply voltage node for the LinkSwitch-TNZ. When the MOSFET is on, the LinkSwitch-TNZ runs off of the energy stored in the bypass capacitor. Extremely low power consumption of the internal circuitry allows the LinkSwitch-TNZ to operate continuously from the current drawn from the DRAIN pin. A bypass capacitor value of 0.1 µF is sufficient for both high frequency decoupling and energy storage. In addition, there is a shunt regulator clamping the BYPASS pin at $V_{BP(SHUNT)}$ (5.2 V) when current is provided to the BYPASS pin through an external resistor. This facilitates powering of LinkSwitch-TNZ externally through a bias winding to decrease the no-load consumption to about 10 mW (flyback). The device stops switching instantly and enters auto-restart when a current $\geq I_{BPSD}$ is delivered into the BYPASS pin. Adding an external Zener diode from the output voltage to the BYPASS pin allows implementing an hysteretic OVP function in a flyback converter (see Figure 6). The current into the BYPASS pin should be limited to less than 16 mA.

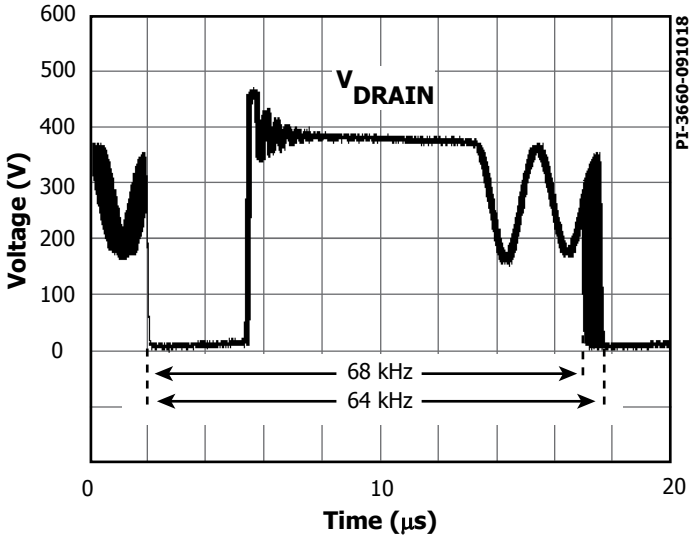


Figure 5. Frequency Jitter.

BYPASS Pin Undervoltage

The BYPASS pin undervoltage circuitry disables the power MOSFET when the BYPASS pin voltage drops below V_{BP}–V_{BPH} (approximately 4.5 V). Once the BYPASS pin voltage drops below this threshold, it must rise back to V_{BP} to enable (turn-on) the power MOSFET.

Over-Temperature Protection

The thermal shutdown circuitry senses the die temperature. The threshold is set at T_{SD} (142 °C typical) with a 75 °C (T_{SDH}) hysteresis. When the die temperature rises above T_{SD} the power MOSFET is disabled and remains disabled until the die temperature falls to T_{SD}–T_{SDH}, at which point it is re-enabled.

Current Limit

The current limit circuit senses the current in the power MOSFET. When this current exceeds the internal threshold (I_{LIMIT}), the power MOSFET is turned off for the remainder of that cycle. The leading edge blanking circuit inhibits the current limit comparator for a short time (t_{LEB}) after the power MOSFET is turned on. This leading edge blanking time has been set so that current spikes caused by capacitance and rectifier reverse recovery time will not cause premature termination of the switching pulse. Current limit can be selected using the BYPASS pin capacitor (0.1 µF for normal current limit / 1 µF for reduced current limit). LinkSwitch-TNZ selects between normal and reduced current limit at power-up prior to switching.

Auto-Restart

In the event of a fault condition such as output overload, output short, or an open-loop condition, LinkSwitch-TNZ enters into auto-restart operation. An internal counter clocked by the oscillator gets reset every time the FEEDBACK pin is pulled high. If the FEEDBACK pin is not pulled high for $t_{AR(ON)}$ (50 ms), the power MOSFET switching is disabled for a time equal to the auto-restart off-time. The first time a fault is asserted the off-time is 150 ms ($t_{AR(OFF)}$ First Off Period). If the fault condition persists, subsequent off-times are 1500 ms long ($t_{AR(OFF)}$ Subsequent Periods). The auto-restart alternately enables and disables the switching of the power MOSFET until the fault condition is removed. The auto-restart counter is gated by the switch oscillator.

Hysteretic Output Overvoltage Protection

The output overvoltage protection provided by the LinkSwitch-TNZ IC uses auto-restart that is triggered by a current >I_{BPSD} into the BYPASS pin. In addition to an internal filter, the BYPASS pin capacitor forms an external filter providing noise immunity from inadvertent triggering. For the bypass capacitor to be effective as a high frequency filter, the capacitor should be located as close as possible to the SOURCE and BYPASS pins of the device.

The OVP function can be realized in a flyback converter by connecting a Zener diode from the output supply to the BYPASS pin. The circuit example shown in Figure 6 describes a simple method for implementing the output overvoltage protection. Adding additional filtering can be achieved by inserting a low value (10 Ω to 47 Ω) resistor in series with the OVP Zener diode. The resistor in series with the OVP Zener diode also limits the maximum current into the BYPASS pin. The current should be limited to less than 16 mA.

During a fault condition resulting from loss of feedback, the output voltage will rapidly rise above the nominal voltage. A voltage at the output that exceeds the sum of the voltage rating of the Zener diode connected from the output to the BYPASS pin and bypass voltage, will cause a current in excess of I_{BPSD} injected into the BYPASS pin, which will trigger the auto-restart and protect the power supply from overvoltage.

Line Overvoltage Protection

In a flyback converter LinkSwitch-TNZ can sense indirectly the DC bus overvoltage condition during the power MOSFET on-time by monitoring the current flowing into the FEEDBACK pin depending on circuit configuration. Figure 7 shows one possible circuit implementation. During the MOSFET on-time, the voltage across the secondary winding is proportional to the voltage across the primary winding. The current flowing through emitter and base of transistor Q3 is therefore representing V_{BUS}. Indirect line sensing minimizes power dissipation and is used for line OV protection. The LinkSwitch-TNZ will go into auto- auto-restart mode if the FEEDBACK pin current exceeds the line overvoltage threshold current I_{FBSD} for at least 2 consecutive switching cycles.

In order to have accurate line OV threshold voltage and also for good efficiency, regulation performance and stability, the transformer leakage inductance should be minimized. Low leakage will minimize ringing on the secondary winding and provide accurate line OVP sampling. In some designs, a RC snubber across the rectifier diode may be needed to damp the ringing at the secondary winding when line voltage is sampled.

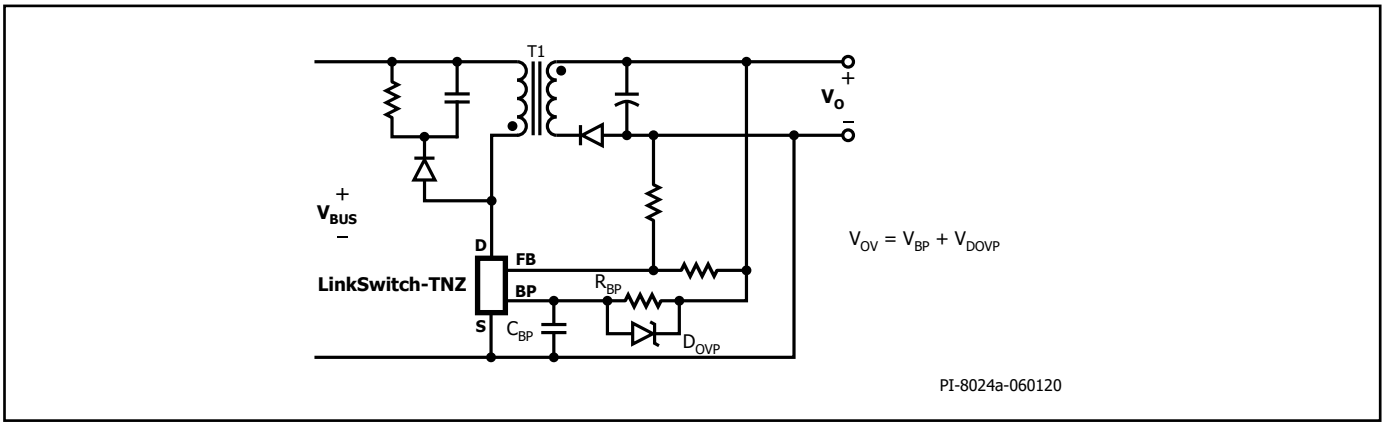


Figure 6. Non-Isolated Flyback Converter with Output Overvoltage Protection (Z1/Z2 Circuitry Not Shown for Clarity).

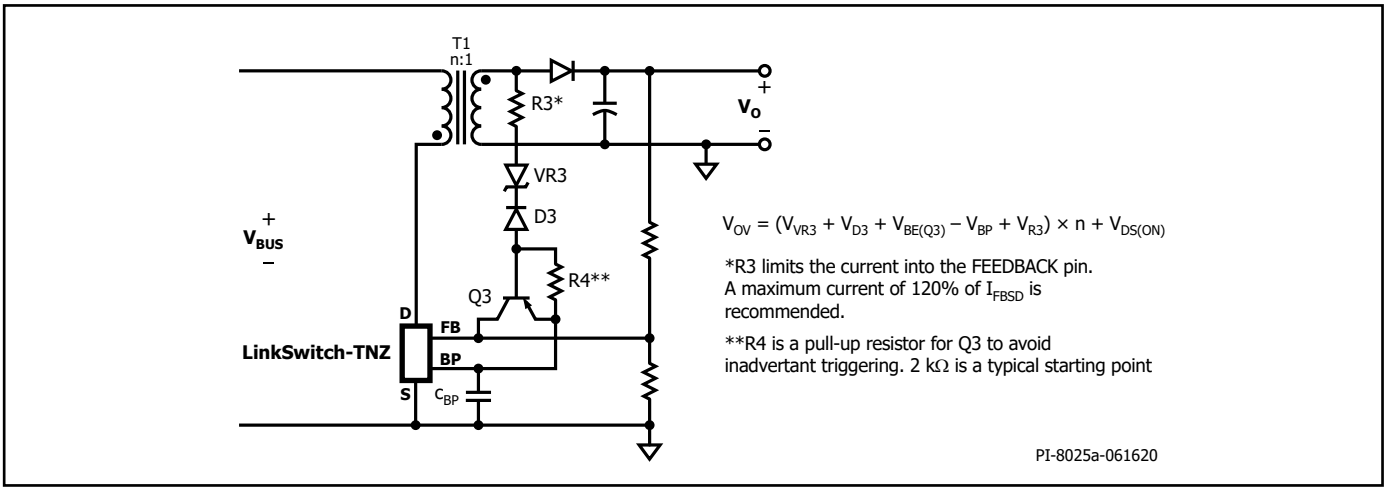


Figure 7. Line-Sensing for Overvoltage Protection by Using FEEDBACK Pin (Z1/Z2 Circuitry Not Shown for Clarity).

ON/OFF Operation with Current Limit State Machine

The internal clock of the LNK33x7 runs all the time. At the beginning of each clock cycle, it samples the FEEDBACK pin to decide whether or not to implement a switch cycle, and based on the sequence of samples over multiple cycles, it determines the appropriate current limit. At high loads, the state machine sets the current limit to its highest value. At lighter loads, the state machine sets the current limit to reduced values.

At near maximum load, LNK33x7 will conduct during nearly all of its clock cycles (Figure 8). At slightly lower load, it will "skip" additional cycles in order to maintain voltage regulation at the power supply output (Figure 9). At medium loads, cycles will be skipped and the current limit will be reduced (Figure 10). At very light loads, the current limit will be reduced even further (Figure 11). Only a small percentage of cycles will occur to satisfy the power consumption of the power supply.

The response time of the ON/OFF control scheme is very fast compared to PWM control. This provides tight regulation and excellent transient response.

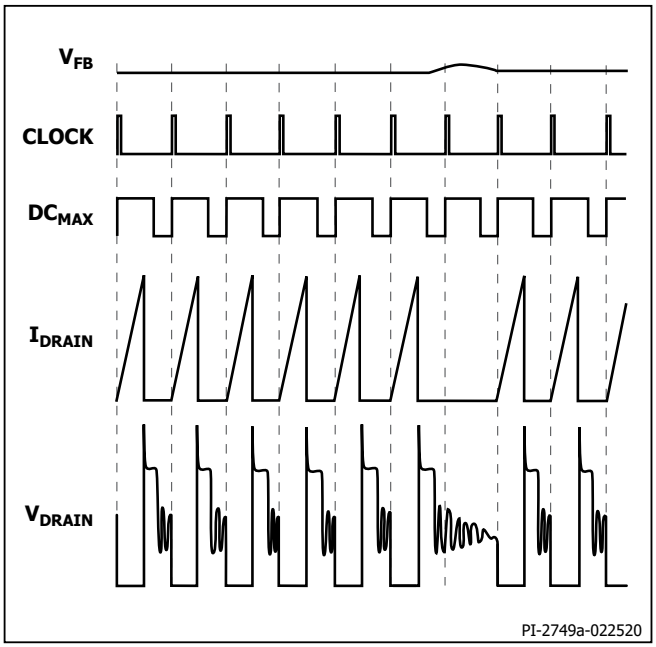


Figure 8. Operation at Near Maximum Loading (Flyback).

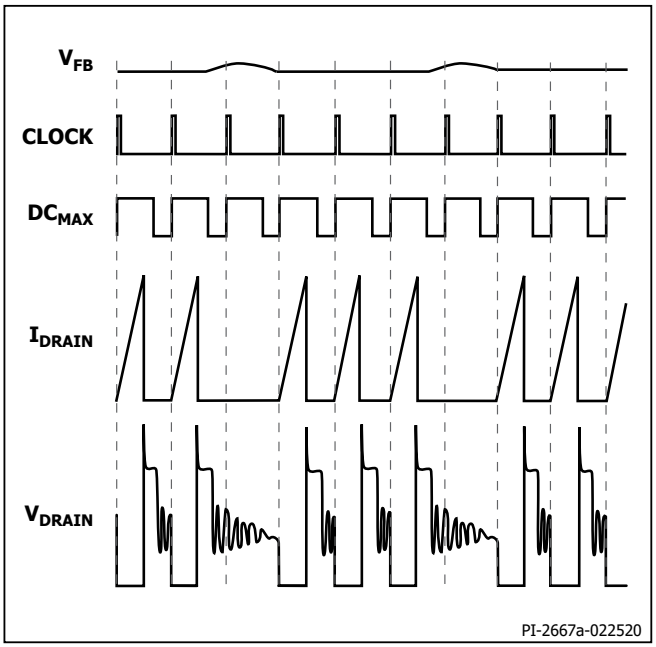


Figure 9. Operation at Moderately Heavy Loading (Flyback).

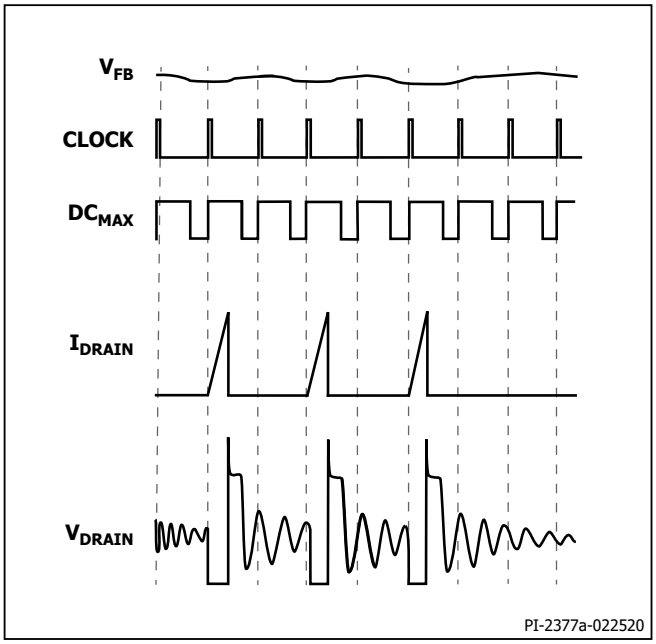


Figure 10. Operation at Medium Loading (Flyback).

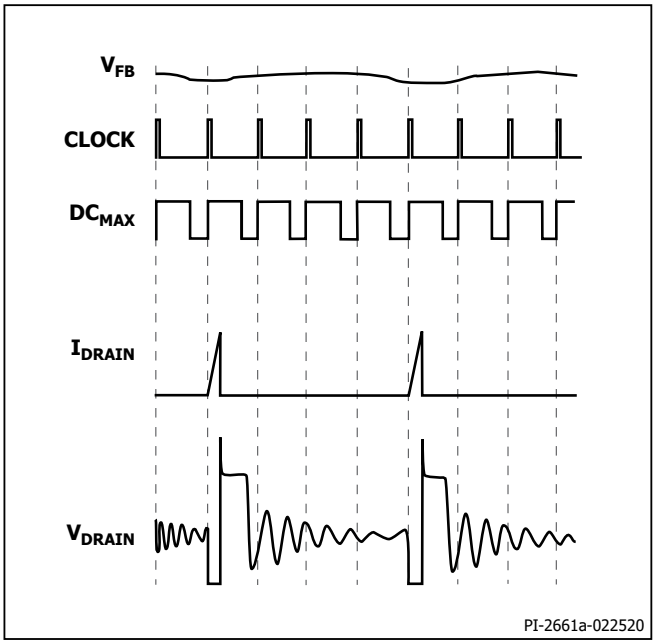


Figure 11. Operation at Very Light Load (Flyback).

Applications Example

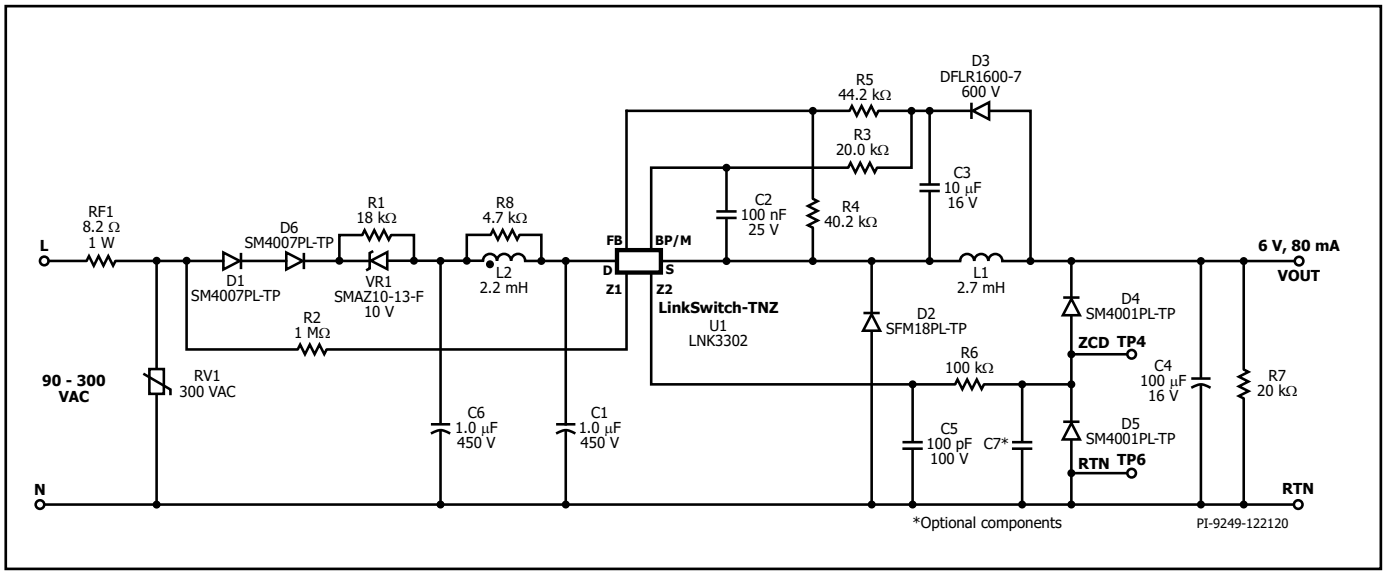


Figure 12. Universal Input, 6 V, 80 mA Constant Voltage Power Supply with Zero-Crossing Detector using LinkSwitch-TNZ.

A 0.48 W Universal Input Buck Converter

The circuit shown in Figure 12 is a typical implementation of a 6 V, 80 mA non-isolated power supply used in 2-wire smart switch applications.

The input stage comprises of fusible resistor RF1, varistor RV1, diodes D1 and D6, capacitors C1 and C6, inductor L2 with resistor R8, and the R-Z circuit R1 and VR1. Resistor RF1 is a flame-proof, fusible, wire-wound resistor. It accomplishes several functions:

A. Inrush current limitation to safe levels for rectifiers D1 and D6;
B. Differential mode noise attenuation;
C. Acts as an input fuse in the event any other component fails short-circuit (component fails safely open-circuit without emitting smoke, fire or incandescent material).

RV1 is added for surge protection. The R-Z circuit minimizes the no-load input current by putting a large series resistance R1 which increases the system power factor. The Zener diode clamps the voltage across R1 during startup and at higher output load.

D1 and D6 provide rectification as well as protection during ring-wave surge which is typically tested above 2 kV. In order to avoid a phase shift during ZCD measurement, it is not recommended to place one of the diodes on the Neutral side.

The power processing stage is formed by LinkSwitch-TNZ U1, freewheeling diode D2, output choke L1, and output capacitor C4. LNK3302 was selected such that the power supply operates in mostly continuous conduction mode (CCM). Diode D2 is an ultrafast diode with a reverse recovery time (t_{RR}) of 35 ns recommended for CCM operation. For mostly discontinuous conduction mode (MDCM) designs, a diode with a t_{RR} of 75 ns is acceptable. Inductor L1 is a standard off-the-shelf inductor with appropriate RMS current rating. Capacitor C4 is a low-ESR electrolytic capacitor to minimize the output voltage ripple. A small pre-load R7 is required to limit the output voltage to about 110% of the rated voltage during light load or no-load condition.

Capacitor C2 with a value of 100 nF sets the current limit to Standard mode. Resistor R3 provides an external current supply to the BYPASS (BP) pin to lower the no-load input power.

To a first order, the forward voltage drops of D2 and D3 are identical. Therefore, the voltage across C3 tracks the output voltage. The voltage developed across C3 is sensed and regulated via the resistor divider R4 and R5 connected to U1's FEEDBACK pin. The values of R4 and R5 are selected such that, at the desired output voltage, the voltage at the FEEDBACK pin is 2 V.

Regulation is maintained by skipping switching cycles. As the output voltage rises, the current into the FEEDBACK pin will rise. If this exceeds I_{FB} then subsequent cycles will be skipped until the current reduces below I_{FB}. Thus, as the output load is reduced, more cycles will be skipped and if the load increases, fewer cycles are skipped. To provide overload protection if no cycles are skipped during a 50 ms period, LinkSwitch-TNZ will enter auto-restart, limiting the average output power to approximately 3% of the maximum overload power.

Z1 and Z2 pins are configured to provide a lossless (<5 mW) zero crossing detection (ZCD) circuit. Z2 is connected to one of the input AC lines through resistor R2 while Z1 forms the ZCD signal output.

When the AC voltage is more positive with respect to Neutral, D4 is forward-biased and clamps ZCD output to VOUT + 0.7 V. At the negative-going phase of the AC input, D5 is forward-biased and clamps ZCD output to -0.7 V.

The passive components comprised of R2, C5, R6, and optional C7 provide noise filtering to ensure clean ZCD signal. The values are chosen such that the overall ZCD delay is kept below 200 µs. C7 is a placeholder for the additional filter if needed. D5 has capacitance that helps avoid adding the extra capacitor. However, care must be taken when selecting the diode since too much capacitance will cause more delay.

Key Application Considerations

LinkSwitch-TNZ Design Considerations

Output Current Table (Buck Topology)
Table 1 represents the typical practical continuous output current that LinkSwitch-TNZ can deliver under the following assumptions:

1. Buck topology.
2. The minimum DC input voltage is ≥70 V. The value of input capacitance should be large enough to meet this criterion.
3. For CCM operation a KRP* of 0.4.
4. 12 VDC output voltage.
5. 75% efficiency.
6. A catch/freewheeling diode with t_{RR} ≤75 ns is used for MDCM operation and for CCM operation, a diode with t_{RR} ≤35 ns is used.
7. The part is board mounted with SOURCE pins soldered to a sufficient area of copper to keep the SOURCE pin temperature at or below 110 °C.

*KRP is the ratio of ripple to peak inductor current.

Output Power Table (Flyback Topology)
Table 2 represents the maximum practical continuous power that LinkSwitch-TNZ can deliver under the following assumptions:

1. Flyback topology.
2. 12 VDC output voltage.
3. 75% efficiency.
4. CCM operation with KRP of 0.6.
5. Open frame, 25 °C ambient.
6. The part is board-mounted with SOURCE pins soldered to a sufficient area of copper to keep the SOURCE pin temperature at or below 110 °C.

LinkSwitch-TNZ Selection and Selection Between MDCM and CCM Operation

Select the LinkSwitch-TNZ device, freewheeling diode and output inductor that gives the lowest overall cost. In general, MDCM provides the lowest cost and highest efficiency converter. CCM designs require a larger inductor and ultrafast (t_{RR} ≤35 ns) freewheeling diode in all cases. It is lower cost to use a larger LinkSwitch-TNZ in MDCM than a smaller LinkSwitch-TNZ in CCM because of the additional external component costs of a CCM design. However, if the highest output current is required, CCM should be employed following the guidelines below.

Topology Options
LinkSwitch-TNZ can be used in all common topologies, with or without an optocoupler and reference to improve output voltage tolerance and regulation. Table 2 provides a summary of these configurations. For more information see the Application Note – LinkSwitch-TNZ Design Guide.

Component Selection

Referring to Figure 12, the following considerations may be helpful in selecting components for a LinkSwitch-TNZ design.

BYPASS Pin Capacitor C2
Capacitor connected from the BYAPSS pin provides decoupling for the controller and also selects current limit. A 0.1 µF or 1 µF capacitor may be used as indicated in the data sheet. Though electrolytic capacitors may be used, surface mount multi-layer ceramic capacitors are preferred for use as they enable placement of capacitors close to the IC and design of compact switching power supplies. 16 V, 25 V or higher X7R dielectric capacitors are recommended to ensure minimum capacitance change under DC bias and temperature.

Freewheeling Diode D2
Diode D2 should be an ultrafast type. For MDCM, reverse recovery time t_{RR} ≤75 ns should be used at a temperature of 70 °C or below. Slower diodes are not acceptable, as continuous mode operation will always occur during startup, causing high leading edge current spikes, terminating the switching cycle prematurely, and preventing the output from reaching regulation. If the ambient temperature is above 70 °C then a diode with t_{RR} ≤35 ns should be used.

For CCM an ultrafast diode with reverse recovery time t_{RR} ≤35 ns should be used. A slower diode may cause excessive leading edge current spikes, terminating the switching cycle prematurely and preventing full power delivery.

Fast recovery and slow recovery diodes should never be used as the large reverse recovery currents can cause excessive power dissipation in the diode and/or exceed the maximum drain current specification of LinkSwitch-TNZ.

Feedback Diode D3
Diode D3 can be a low-cost slow diode such as the 1N400X series, however it should be specified as a glass passivated type to guarantee a specified reverse recovery time. To a first order, the forward drops of D2 and D3 should match.

Inductor L1
Choose any standard off-the-shelf inductor that meets the design requirements. A "drum" or "dog bone" "I" core inductor is recommended with a single ferrite element due to its low-cost. Minimize audible noise by varnishing the inductor. The typical inductance value and RMS current rating can be obtained from the LinkSwitch-TNZ design spreadsheet available within the PI Expert design suite from Power Integrations. Choose L1 greater than or equal to the typical calculated inductance with RMS current rating greater than or equal to calculated RMS inductor current.

Output Capacitor C4
The primary function of capacitor C4 is to smooth the inductor current. The actual output ripple voltage is a function of this capacitor's ESR. To a first order, the ESR of this capacitor should not exceed the rated ripple voltage divided by the typical current limit of the chosen LinkSwitch-TNZ.

Feedback Resistors R4 and R5
The values of the resistors in the resistor divider formed by R4 and R5 are selected to maintain 2 V at the FEEDBACK pin.

External Bias Resistor R3
To reduce the no-load input power of the power supply, resistor R3, connected from the feedback capacitor C3 to the BYPASS pin, is recommended. This is applicable to the power supply whose output voltage is higher than $V_{BP(SHUNT)}$. To achieve lowest no-load power consumption, the current fed into the BYPASS pin should be slightly higher than I_{S1}. For the best full-load efficiency and thermal performance, the current fed into the BYPASS pin should be slightly higher than the I_{S2} Max value.

Feedback Capacitor C3
Capacitor C3 can be a low-cost general purpose capacitor. It provides a "sample and hold" function, charging to the output voltage during the off time of LinkSwitch-TNZ. Its typical value is 10 µF.

Pre-Load Resistor R7
In high-side, direct-feedback, a pre-load resistor is required to maintain output regulation at light or no-load. The value of R7 should be selected to provide a balance between power loss and output regulation.

ZCD Circuit

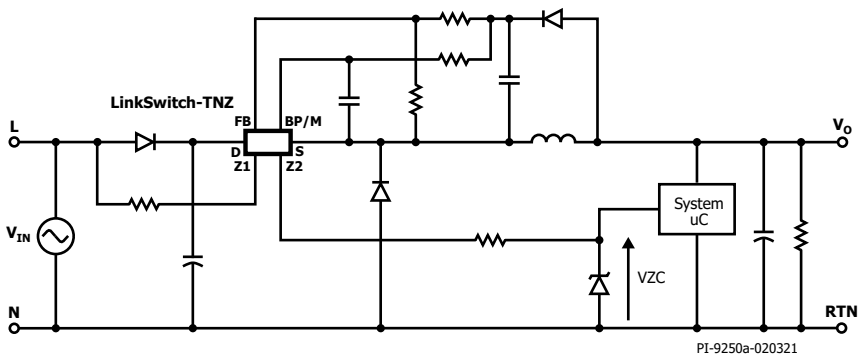
The ZCD configuration shown in Figure 12 is just one of the various options that the user can choose based on topology selection. In high-side buck configuration, Z1/Z2 pins are more prone to switching-noise coupling especially at high-line, full-load due to floating SOURCE pin. Unmitigated noise may affect not only the ZCD signal but also cause higher conducted emission. Resistor R2 should be large enough to minimize the impact on EMI while keeping the ZCD delay to an acceptable level. A network of filters composed of C5, R6 and an optional C7 (<100 pF) are needed to ensure clean ZCD signal. For D5, choose a diode with junction capacitance of <100 pF.

X Capacitor Discharge (LNK331x Only)

X capacitor discharge function can be implemented by connecting Z1 to one AC line input through an external series resistor and Z2 to the other AC input line input through a separate external resistor. Nominal values of total X capacitance and series resistor range (RC time constant is <1 second) is shown in the table below.

Total X Capacitance	Total Series Resistance
100 nF to 6 μF	7.5 MΩ to 142 kΩ

Non-Isolated Configurations



- Output referenced to Neutral
- Positive output voltage relative to Neutral
- Step down – $V_O < V_{IN}$
- Low-cost direct feedback (±5% typ.)
- Requires an output load to maintain regulation
- ZCD signal toggles every half-line AC cycle
- ZCD logic follows the AC line
- Lowest ZCD component count
- Higher Zener diode capacitance may affect ZCD delay
- ZCD low signal is -0.7 V with respect to system GND
- X capacitor discharge capable

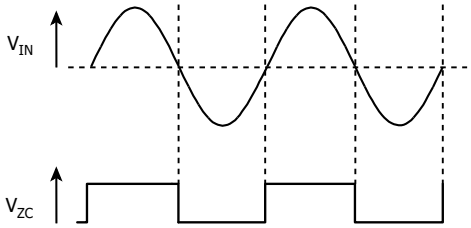
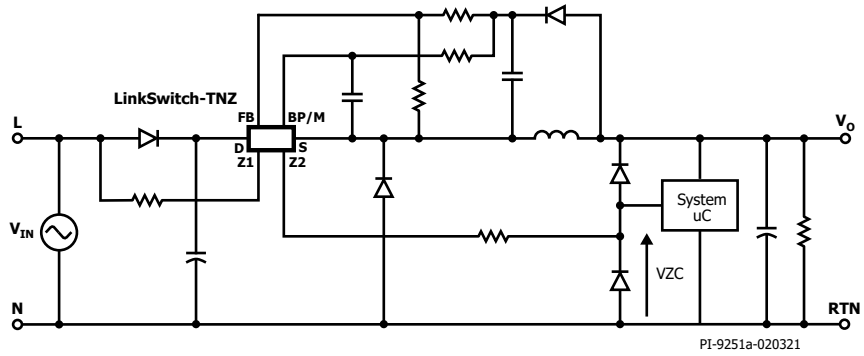


Figure 13. High-Side Buck, Half-Wave Rectification ZCD with Zener Diode.



- Output referenced to Neutral
- Positive output voltage relative to Neutral
- Step down – $V_O < V_{IN}$
- Low-cost direct feedback (±5% typ.)
- Requires an output load to maintain regulation
- ZCD signal toggles every half-line AC cycle
- ZCD logic follows the AC line
- Typically has faster ZCD slew rate due to lower capacitance than Zener
- ZCD low signal is -0.7 V with respect to system GND
- Not configured for X capacitor discharge

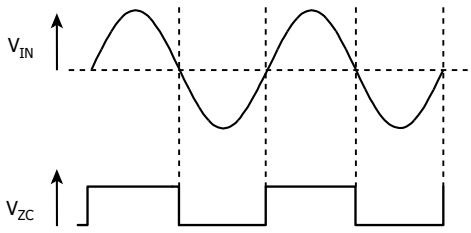
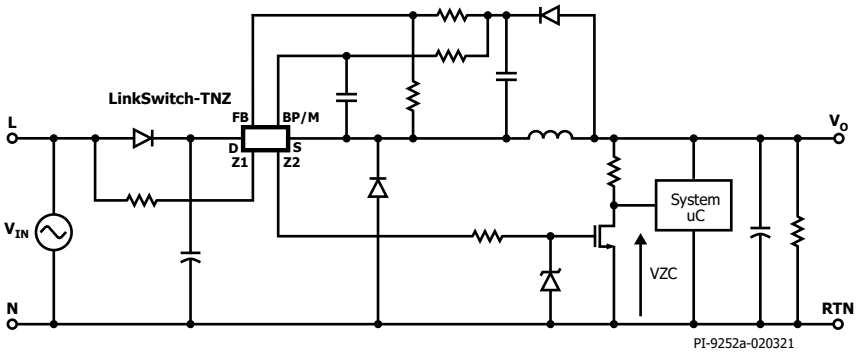


Figure 14. High-Side Buck, Half-Wave Rectification ZCD with 2 Diodes.



- Output referenced to Neutral
- Positive output voltage relative to Neutral
- Step down – $V_O < V_{IN}$
- Low-cost direct feedback (±5% typ.)
- Requires an output load to maintain regulation
- ZCD signal toggles every half-line AC cycle
- Inverted ZCD logic with respect to AC line
- ZCD logic low signal is the same as system GND
- X capacitor discharge capable

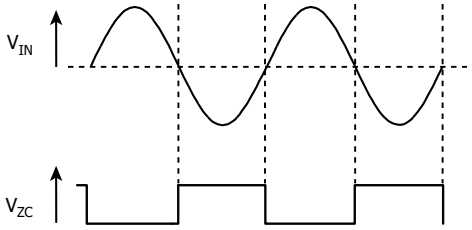
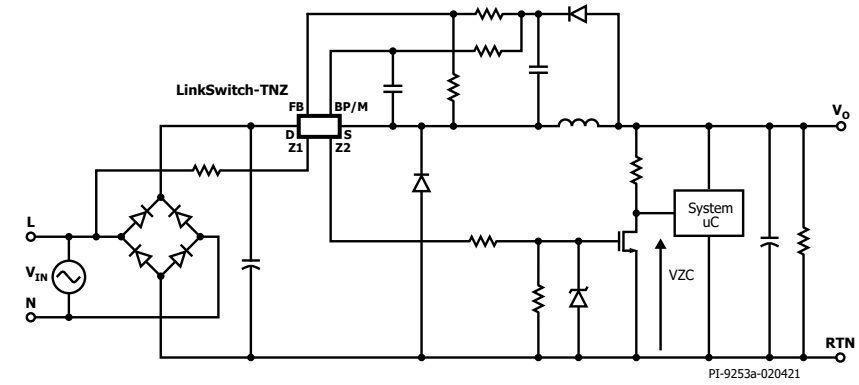


Figure 15. High-Side Buck, Half-wave Rectification ZCD with MOSFET.



- Positive output voltage relative to Neutral
- Step down – $V_O < V_{IN}$
- Low-cost direct feedback (±5% typ.)
- Requires an output load to maintain regulation
- Higher power capability than half-wave rectifier
- ZCD signal toggles every half-line AC cycle
- Inverted ZCD logic with respect to AC line
- ZCD low signal is the same as system GND
- ZCD signal probing requires special setup in order to prevent signal disruption
- Not configured for X capacitor discharge

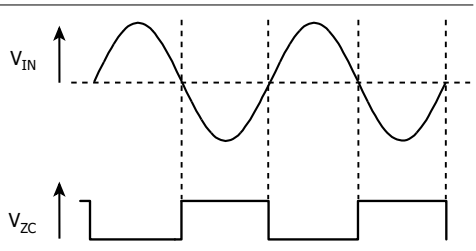
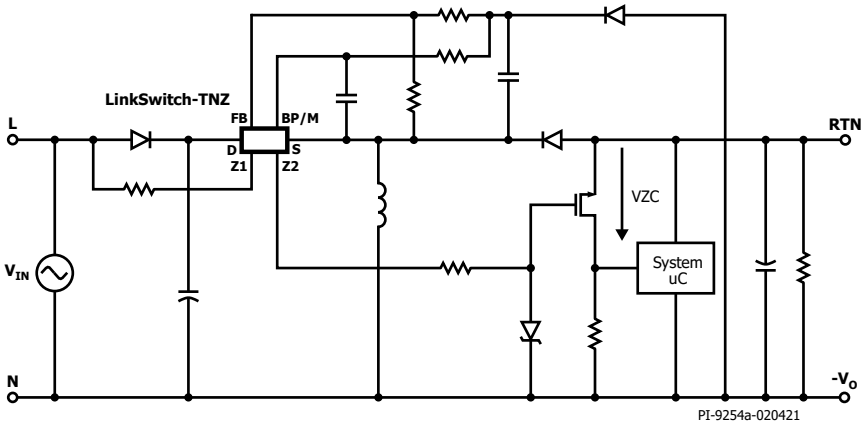


Figure 16. High-Side Buck, Bridge Rectifier, ZCD with MOSFET.



- Negative output voltage relative to Neutral
- Step up/down – $V_O > V_{IN}$ or $V_O < V_{IN}$
- Low-cost direct feedback (±5 % typ.)
- Fail-safe – output is not subjected to input voltage if the internal power MOSFET fails
- Requires an output load to maintain regulation
- ZCD signal toggles every half-line AC cycle
- Inverted ZCD logic with respect to AC line
- X capacitor discharge capable

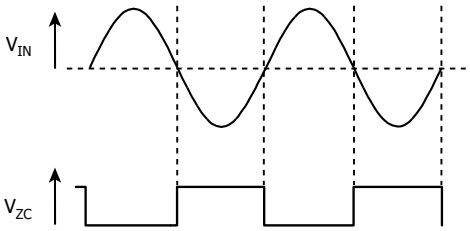
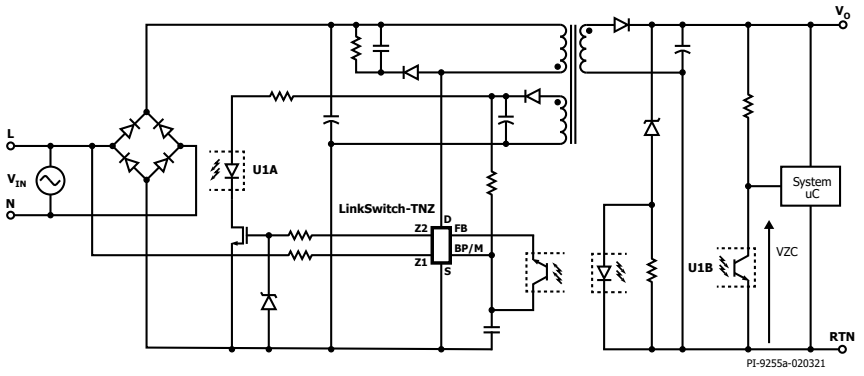


Figure 17. High-Side Buck-Boost with Direct Feedback.



- Step up/down – $V_O > V_{IN}$ or $V_O < V_{IN}$
- Opto-coupler feedback
- Does not require a pre-load
- ZCD signal toggles every half-line AC cycle
- Inverted ZCD logic with respect to AC line
- ZCD signal referenced to Secondary
- Not configured for X capacitor discharge

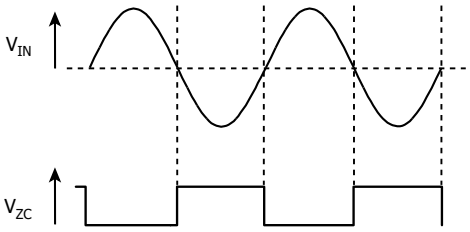
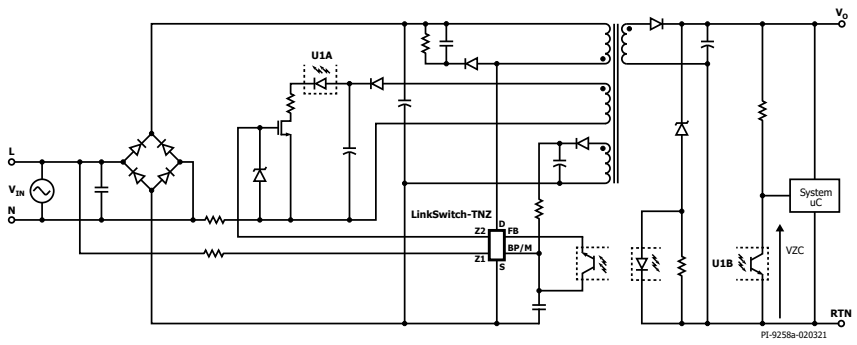


Figure 18. Isolated Flyback with AUX Winding for IC Bias.



- Step up/down – $V_O > V_{IN}$ or $V_O < V_{IN}$
- Opto-coupler feedback
- Does not require a pre-load
- ZCD signal toggles every half-line AC cycle
- Inverted ZCD logic with respect to AC line
- ZCD signal referenced to Secondary
- Requires additional bias winding referenced to Neutral
- X capacitor discharge capable

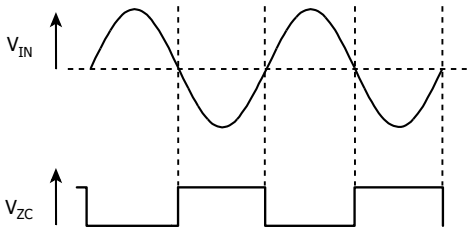
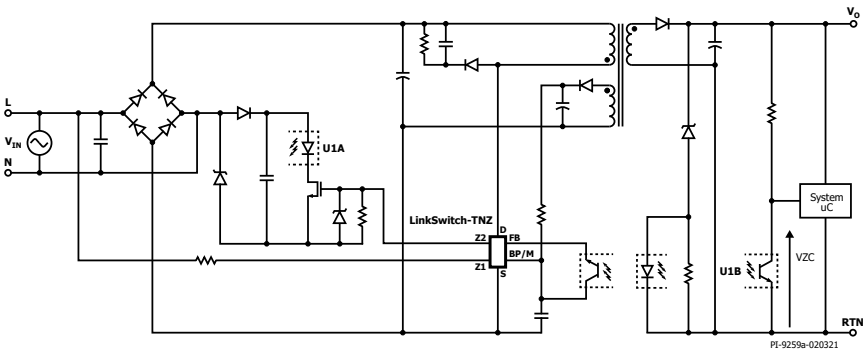


Figure 19. Isolated Flyback with Dedicated Winding for ZCD Optocoupler Bias.



- Step up/down – $V_O > V_{IN}$ or $V_O < V_{IN}$
- Opto-coupler feedback
- Does not require a pre-load
- ZCD signal triggers every AC line period
- Inverted ZCD logic with respect to AC line
- ZCD signal referenced to Secondary
- X capacitor discharge capable

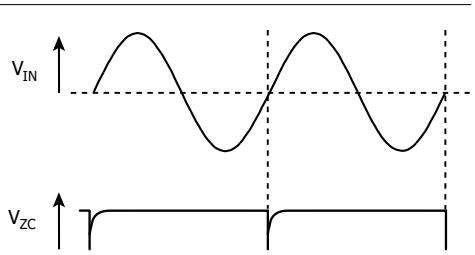


Figure 20. Isolated Flyback with Self-Biased ZCD Optocoupler.

LinkSwitch-TNZ Layout Considerations

In the buck or buck-boost converter configuration, since the SOURCE pins in LinkSwitch-TNZ are switching nodes, the copper area connected to SOURCE should be minimized to minimize EMI within the thermal constraints of the design.

In the boost configuration, since the SOURCE pins are tied to DC return, the copper area connected to SOURCE can be maximized to improve heat sinking.

Figure 21 is printed circuit board layout design examples for the circuit schematic shown in Figure 12. The loop formed between the LinkSwitch-TNZ U1, freewheeling diode D2, and input capacitor C1 should be kept as small as possible. The BYPASS pin capacitor C2 should be located physically close to the SOURCE (S) and BYPASS (BP) pins. To minimize direct coupling from switching nodes, the LinkSwitch-TNZ should be placed away from AC input lines.

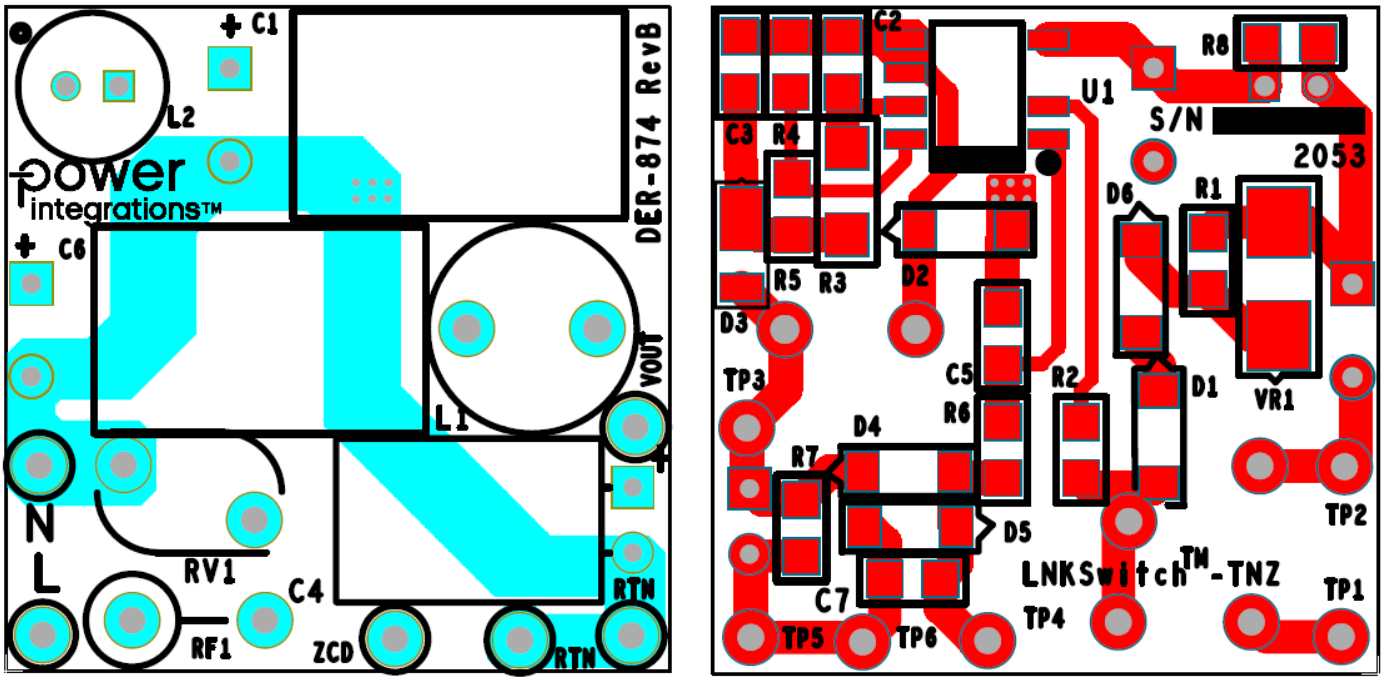


Figure 21. Example Printed Circuit Layout for LinkSwitch-TNZ High-Side Buck Configuration.

Safety Considerations

Based on UL/IEC 60950 safety standard, functional insulation can be met by satisfying any of these conditions:

1. Creepage and clearance requirements for functional insulation.
2. Withstand electric strength tests for functional insulation.
3. Short-circuited and there is no overheating of any material creating a risk of fire, no emission of molten material, no opening of PCB trace, and the temperature is within limits.

Z1 and Z2 pins functional safety compliance falls under condition 3 - i.e., even if the pins are shorted, there will be no risk of Safety violation as long as the external components (resistors, capacitors) are rated properly.

Quick Design Checklist

As with any power supply design, all LinkSwitch-TNZ designs should be verified for proper functionality on the bench. The following minimum tests are recommended:

1. Adequate DC Rail Voltage – Check that the minimum DC input voltage does not fall below 70 VDC at maximum load, minimum input voltage.
2. Correct Diode Selection – UF400x series diodes with reverse recovery time of 75 ns or better are recommended only for designs that operate in MDCM at an ambient of 70 °C or below. For designs operating in continuous conduction mode (CCM) and/or higher ambients, then a diode with a reverse recovery time of 35 ns or better, such as the BYV26C, is recommended.
3. Maximum Drain Current – Verify that the peak drain current is below the data sheet peak drain specification under worst-case conditions of highest line voltage, maximum overload (just prior to auto-restart) and highest ambient temperature.
4. Thermal check – At maximum output power, minimum input voltage and maximum ambient temperature, verify that the LinkSwitch-TN2 SOURCE pin temperature is 100 °C or below. This ensures adequate margin due to variations in $R_{DS(ON)}$ from part to part. If the device temperature of the IC exceeds 85 °C with ambient temperature of 25 °C, it is recommended the next bigger device in the family should be selected for the application. A battery powered thermocouple meter is recommended to make measurements when the SOURCE pins are a switching node. Alternatively, the ambient temperature may be raised to indicate margin to thermal shutdown.

In a LinkSwitch-TNZ design using a buck or buck-boost converter topology, the SOURCE pin is a switching node. Oscilloscope measurements should therefore be made with probe grounded to a DC voltage, such as primary return or DC input rail, and not to the SOURCE pins. The power supply input must always be supplied from an isolated source when doing measurements (e.g. via an isolation transformer).

Absolute Maximum Ratings[1,5]

DRAIN Pin Voltage: LNK33xx ..... -0.3 V to 725 V
DRAIN Pin Peak Current: LNK33x2 ..... 600 mA[2]
LNK33x4 ..... 1230 mA[2]
LNK33x6/7 ..... 3750 mA[2]
Z1/Z2 Pin Voltage[6]: LNK33xx ..... 1000 V
Z1/Z2 Pin Current[7]: LNK33xx ..... 5 mA
FEEDBACK Pin Current ..... 100 mA
FEEDBACK Pin Voltage ..... -0.3 V to 7 V
BYPASS Pin Voltage ..... -0.3 V to 7 V
Storage Temperature ..... -65 to 150 °C
Operating Junction Temperature[3] ..... -40 to 150 °C
Lead Temperature[4] ..... 260 °C

NOTES:

1. All voltages referenced to SOURCE, T_A = 25 °C.
2. See Figure 15 and Figure 25 for V_{DS} > 400 V.
3. Normally limited by internal circuitry.
4. 1/16 in. from case for 5 seconds.
5. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect product reliability.
6. Voltage of Z1 pin relative to Z2 pin in either polarity.
7. The peak current is allowed while the Z1/Z2 voltage is simultaneously less than 400 V.

Thermal Resistance

Thermal Resistance:
(θ_{JA}) ..... 100 °C/W[2], 90 °C/W[3]
(θ_{JC})[1] ..... 30 °C/W

Notes:

1. Measured on pin 8 (SOURCE) close to plastic interface.
2. Soldered to 0.36 sq. inch (232 mm^2), 2 oz. (610 g/m^2) copper clad.
3. Soldered to 1 sq. inch (645 mm^2), 2 oz. (610 g/m^2) copper clad.

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Output Frequency	f_{OSC}	T_J = 25 °C	Average	62	66	70	kHz
			Peak-Peak Jitter		4		
Maximum Duty Cycle	DC_{MAX}	T_J = 25 °C		66	69	73	%
FEEDBACK Pin Turnoff Threshold Current	I_{FB}	V_{BPP} = 5.0 V to 5.5 V T_J = 25 °C		44	49	54	µA
FEEDBACK Pin Voltage at Turnoff Threshold	V_{FB}	V_{BPP} = 5.0 V to 5.5 V T_J = 25 °C		1.97	2.00	2.03	V
FEEDBACK Pin Instant Shutdown Current	$I_{FB(SD)}$	T_J = 25 °C		520	675	800	µA
FEEDBACK Pin Instant Shutdown Delay		T_J = 25 °C			2		Switch Cycles
FEEDBACK Pin Voltage at Shutdown Current	$V_{FB(SD)}$	V_{BPP} = 5.0 V to 5.5 V T_J = 25 °C			3.0		V
DRAIN Pin Supply Current	I_{S1}	VFB = 2.1 V (MOSFET Not Switching) See Note A			75		µA
	I_{S2}	FEEDBACK Open (MOSFET Switching) See Notes A, B	LNK33x2		98	160	µA
			LNK33x4		113	180	
			LNK33x6		165	250	
			LNK33x7		190	290	

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions (cont.)							
BYPASS Pin Charge Current	I_{CH1}	V_{BP} = 0 V T_J = 25 °C		-11	-7	-3	mA
	I_{CH2}	V_{BP} = 4 V T_J = 25 °C		-7.5	-5	-2.5	
BYPASS Pin Voltage	V_{BP}			4.7	5.0	5.2	V
BYPASS Pin Shutdown Threshold Current	$I_{BP(SD)}$	T_J = 25 °C			6	8	mA
BYPASS Pin Shunt Voltage	$V_{BP(SHUNT)}$	I_{BP} = 2 mA		4.9	5.2	5.5	V
BYPASS Pin Voltage Hysteresis	$V_{BP(H)}$			0.37	0.47	0.57	V
BYPASS Pin Supply Current	$I_{BP(SC)}$	See Note C		55			µA
Circuit Protection							
Standard Current Limit (C_{BP}) = 0.1 µF See Note D, H	I_{LIMIT}	di/dt = 55 mA/µs T_J = 25 °C	LNK33x2	126	136	146	mA
		di/dt = 250 mA/µs T_J = 25 °C		149	170	191	
		di/dt = 65 mA/µs T_J = 25 °C	LNK33x4	240	257	275	
		di/dt = 415 mA/µs T_J = 25 °C		278	317	356	
		di/dt = 95 mA/µs T_J = 25 °C	LNK33x6	450	482	515	
		di/dt = 610 mA/µs T_J = 25 °C		510	580	650	
		di/dt = 95 mA/µs T_J = 25 °C	LNK33x7	725	780	835	
		di/dt = 610 mA/µs T_J = 25 °C		893	1015	1137	

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Circuit Protection							
Reduced Current Limit (C_{BP}) = 1 µF See Note D, H	$I_{LIMIT(RED)}$	di/dt = 28 mA/µs T_J = 25 °C	LNK33x2	70	80	90	mA
		di/dt = 170 mA/µs T_J = 25 °C		104	119	134	
		di/dt = 65 mA/µs T_J = 25 °C	LNK33x4	180	205	230	
		di/dt = 415 mA/µs T_J = 25 °C		227	258	289	
		di/dt = 95 mA/µs T_J = 25 °C	LNK33x6	325	370	415	
		di/dt = 610 mA/µs T_J = 25 °C		408	464	520	
		di/dt = 95 mA/µs T_J = 25 °C	LNK33x7	545	620	695	
		di/dt = 610 mA/µs T_J = 25 °C		730	830	930	
Minimum On-Time	$t_{ON(MIN)}$	LNK33x2 See Note I		373	534	687	ns
		LNK33x4 See Note I		356	475	594	
		LNK33x6 See Note I		442	591	734	
		LNK33x7 See Note I		656	875	1094	
Leading Edge Blanking Time	t_{LEB}	T_J = 25 °C See Note E		300	450		ns
Thermal Shutdown Temperature	T_{SD}	See Note F		135	142	150	°C
Thermal Shutdown Hysteresis	T_{SDH}	See Note F			75		°C
Internal Soft-Start	$f_{OSC(CC)}$	LNK33xx	Soft-Start Period, See Note E		256		Cycles
			Soft-Start Frequency		33		kHz

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Output							
On-State Resistance	$R_{DS(ON)}$	LNK33x2 I_D = 13 mA	T_J = 25 °C		48	55.2	Ω
			T_J = 100 °C		76	88.4	
		LNK33x4 I_D = 25 mA	T_J = 25 °C		24	27.6	
			T_J = 100 °C		38	44.2	
		LNK33x6 I_D = 45 mA	T_J = 25 °C		7	8.1	
			T_J = 100 °C		11	12.9	
		LNK33x7 I_D = 45 mA	T_J = 25 °C		7	8.1	
			T_J = 100 °C		11	12.9	
Off-State Drain Leakage Current	I_{DSS1}	V_{BP} = 5.4 V V_{FB} ≥2.1 V V_{DS} = 80% BV_{DSS} T_J = 125 °C				200	µA
	I_{DSS2}	V_{BPP} = 5.4 V V_{DSS} = 325 V T_J = 25 °C			15		
Breakdown Voltage	BV_{DSS}	V_{BP} = 5.4 V V_{FB} ≥2.1 V T_J = 25 °C	LNK33xx	725			V
DRAIN Pin Supply Voltage		T_J = 25 °C		18			V
Auto-Restart ON-Time	$t_{AR(ON)}$	T_J = 25 °C See Note G			50		ms
Auto-Restart OFF-Time	$t_{AR(OFF)}$	T_J = 25 °C See Note G	First Off Periods		150		ms
			Subsequent Periods		1500		
Auto-Restart Duty Cycle	DC_{AR}	Subsequent Periods			3		%

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Z1/Z2 Function						
Supply Current	I_{SUPPLY}	T_J = 25 °C			22	µA
Saturation Current (See Note E, J)	I_{DSAT}	LNK331x only	2.5			mA
AC Removal Detection Time	t_{DET}	Line Cycle Frequency 47-63 Hz LNK331x only		22	34	ms

NOTES:

A. Total current consumption is the sum of I_{S1} and I_{DSS} when FEEDBACK pin voltage is = 2.1 V (MOSFET not switching) and the sum of I_{S2} and I_{DSS} when FEEDBACK pin is shorted to SOURCE (MOSFET switching).

B. Since the output MOSFET is switching, it is difficult to isolate the switching current from the supply current at the DRAIN. An alternative is to measure the BYPASS pin current at 5.1 V.

C. This current is only intended to supply an optional optocoupler connected between the BYPASS and FEEDBACK pins and not any other external circuitry.

D. For current limit at other di/dt values, refer to Figures 21 and 22.

E. This parameter is guaranteed by design.

F. This parameter is derived from characterization.

G. Auto-restart on time has the same temperature characteristics as the oscillator (inversely proportional to frequency).

H. The BP/M capacitor value tolerance should be equal or better than indicated below across the ambient temperature range of the target application.

I. Measured using circuit in Figure 12 with 50 Ω drain pull-up. The width of the drain pulse is measured as the time from V_{FALL} = 42 V to V_{RISE} = 40 V (VDR = 50 V), for LNK33x6/x5/x4 and as the time from V_{FALL} = 32 V to V_{RISE} = 30 V on rising edge (VDR = 35 V), for LNK33x2.

J. Saturation current specifications ensure a natural RC discharge characteristic at all voltages up to 265 VAC peak with total external series resistor values 7.5 MΩ to 142 kΩ

Nominal BP/M Pin Capacitor Value	Tolerance Relative to Minimal Capacitor Value	
	Minimum	Maximum
0.1 µF	-60%	+100%
1 µF	-50%	+100%

Recommended to use at least 10 V / 0805 / X7R SMD MLCC.

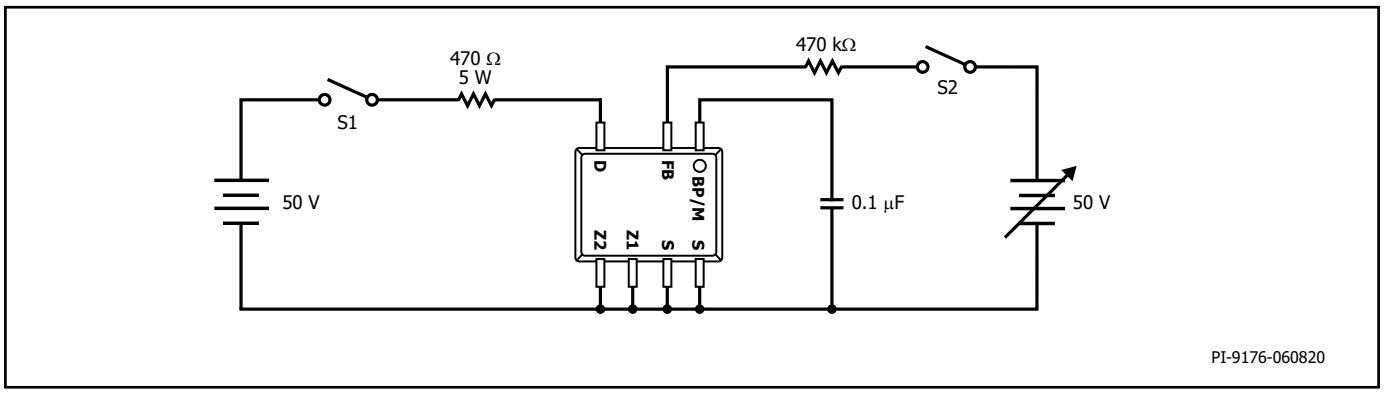


Figure 22. LinkSwitch-TNZ General Test Circuit.

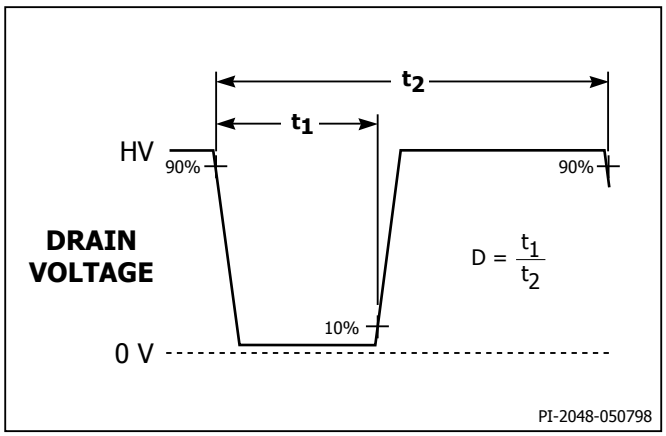


Figure 23. LinkSwitch-TNZ Duty Cycle Measurement.

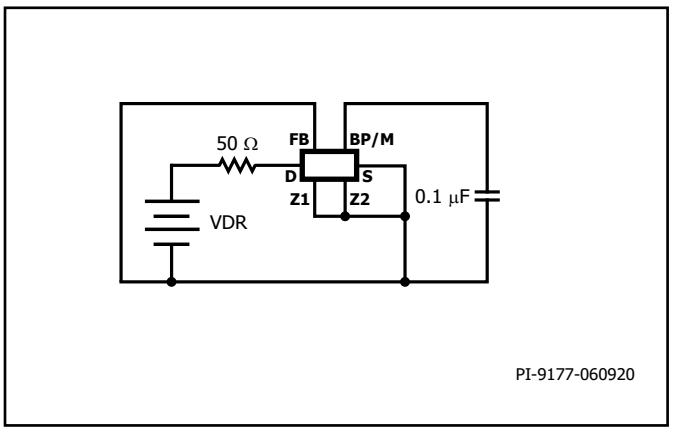


Figure 24. LinkSwitch-TNZ Minimum On-Time Test Circuit.

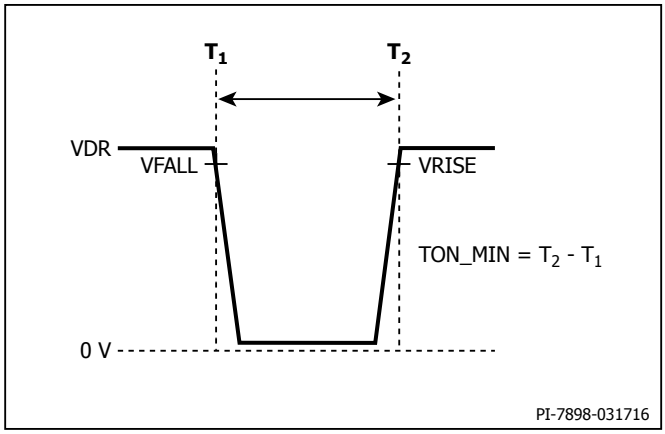
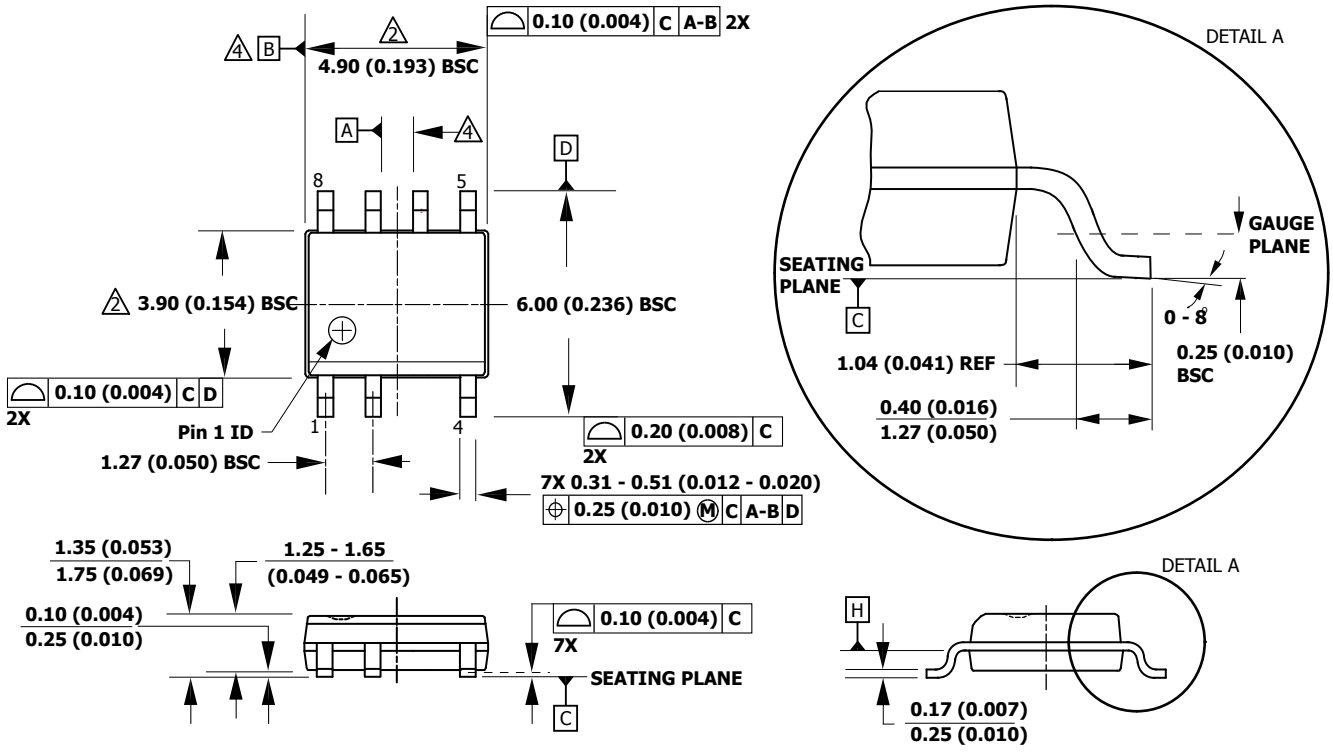


Figure 25. LinkSwitch-TNZ Minimum On-Time Measurement.

SO-8C (D Package)



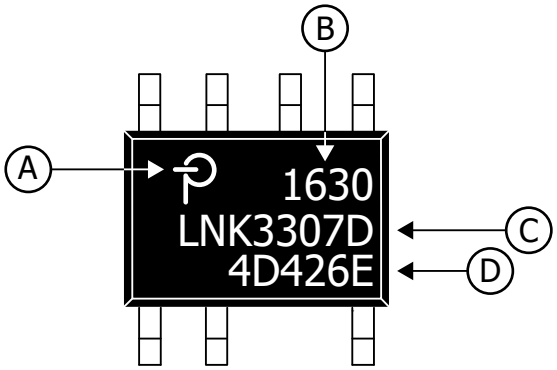
Notes:

1. JEDEC reference: MS-012.
2. Package outline exclusive of mold flash and metal burr.
3. Package outline inclusive of plating thickness.
4. Datums A and B to be determined at datum plane H.
5. Controlling dimensions are in millimeters. Inch dimensions are shown in parenthesis. Angles in degrees.

D07C

PI-4526-012315

SO-8C (D) PACKAGE MARKING



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code

PI-8116c-060220

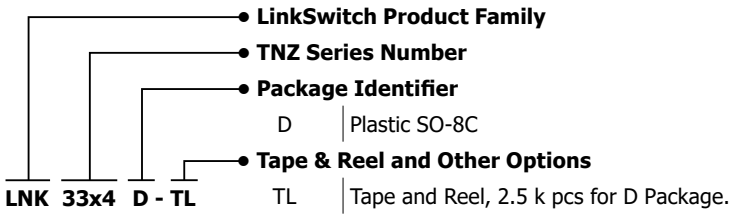
MSL Table

Part Number	MSL Rating
LNK33x2D	3
LNK33x4D	3
LNK33x6D	3
LNK33x7D	3

ESD and Latch-Up Table

Test	Conditions	Results
Latch-up at 125 °C	JESD78D	> ±100 mA or > 1.5 × V_{MAX} on all pins
Human Body Model ESD	ANSI/ESDA/JEDEC JS-001-2014	> ±2 kV on all pins, except DRAIN pin for LNK33x2 ±1.5 kV
Charge Device Model ESD	ANSI/ESDA/JEDEC JS-002-2014	> ±200 V on all pins

Part Ordering Information



Notes

Revision	Notes	Date
B	Code A release.	12/20
C	Added Family part numbers and size 7 parameter updates.	03/21
C	Corrected Diode references in Feedback Diode D3 section on page 7.	05/21
D	Added EN/IEC 62368-1 certification bullet point on page 1.	06/21

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