## General Information

The F/2F Read/Decode Integrated Circuit in intended for use in recovering F/2F encoded data received from a magnetic head.

Features

- 150 to more than 12,000 F/2F bits per second
- Low power: Full operation from 2.4 to 5.5 volts. Current below 2.0 mA.
- Recovers Data with as much as 30% dropout of amplitude.
- Accepts amplitudes from below 20% of ISO reference voltage to more than 250% of ISO reference voltage.
- Meets or exceeds the requirement for:
  - IEC 1000-4-2   ESD (Electro Static Discharge)
  - IEC 1000-4-3   Radiated EMC Field (2x requirement)
  - IEC 1000-4-4   Electrical Fast Transient Burst requirement (transmissions on I/O cable)

Functional Block Diagram
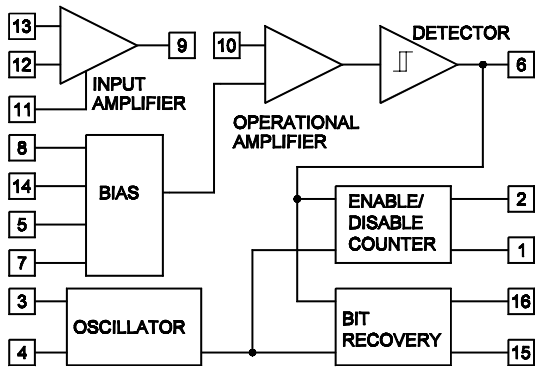
Functional Description

The F/2F Read/Decode I.C. will recover clock and data signals from an F/2F data stream generated from a magnetic head. The I.C. will function for data rates from 150 to more than 12,000 bits per second. Acquisition and tracking of the data within this range is automatic. The F/2F Read/Decode I.C. is composed of three functional sections:

- Signal Conditioning and Detection
- Bit Recovery
- Enable/Disable Counters

The signal conditioning and detection section amplifies and filters the signal from the magnetic head, rejects common mode noise, and detects the signal peaks. Other features include protection against certain waveform distortions that may be present in the signal.

The enable/disable counters provide initialization for the recovery section. These counters initialize both the bit recovery and the signal conditioning and detection sections.

The Bit Recovery section locks onto the data rate and performs the recovery of individual bits from the F/2F data stream.

Absolute Maximum Ratings (Non-Operating)

Supply Voltage ....7.0 Volts
Voltage Input Range.....................0 to VCC
Output Sink Current......................10 mA
Internal Power Dissipation.............100 mW
Storage Temperature Range.........-55 to 150°C
Lead Soldering (10 Sec.)..............260°C

Electrical Characteristics

Unit operates from 2.4 to 5.5 Volts (VCC) and -30° to 70°C
Test conditions: VCC = 5.00 Volts, Ambient Temperature = 25°C

Parameter	Condition	Min.	Max.	Typ.	Units
Device Current			2		mA
Logic Low Out (VOL)	at +2.0 mA [1]		0.4		Volts
Logic High Out (VOH)	at -2.0 mA [1]	VCC - 0.5			Volts
Oscillator Frequency	([2])			1.2	MHz

Table 1: Electrical Characteristics.

Notes:
1. TTL/CMOS compatible. Outputs covered include the following: Card Present, Read Data, Strobe and F/2F.
2. Frequency measured using R2 and C3 component values. Refer to recommended circuit for required values.

Signal Timing Diagram
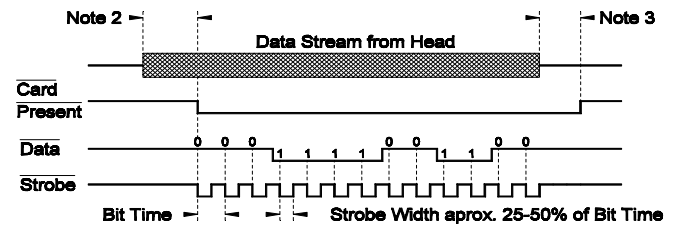
Notes:
1. Card Present, Data, and Strobe are negative true logic.
2. Card Present goes low after 14-15 head flux reversals.
3. Card Present returns to high level approximtely 150mS after the last flux transition.
4. Data is valid 1.0µS (min.) before the leading negative edge of strobe and remains valid until approximately 1.0µS before the next STROBE.

DATA

The DATA signal is valid while the STROBE is low. If the DATA signal is high, the bit is a zero. If the DATA signal is low, the bit is a one.

STROBE

The STROBE signal indicates when DATA is valid. It is recommended that DATA be loaded by the user with the leading negative edge of the STROBE.

CARD PRESENT

CARD PRESENT will go low after 14-15 flux reversals from the head. It will return high if Reset or about 150 milliseconds after the last flux reversal. The CARD PRESENT signal can be tied together with other card present signals from more than one IC, however use only one pull-up resistor (R4). E.g., if this is a 3 track reader, all 3 CARD PRESENTS would be tied together using a single 10K resistor.
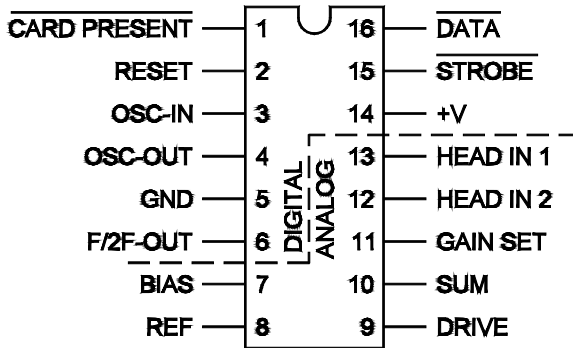
When no card is being moved through the unit, the DATA, STROBE and CARD PRESENT signals are high.

The signal timing diagram shown above represents the data along with other signals that are generated during the reading process.

Reset Feature

In normal operation, the I.C. resets itself approximately 150 milliseconds after the last flux reversal from the magnetic head. Reset may be forced by applying a pulse of 1.0 to 100 microseconds to the RESET pin. The positive edge of the pulse will reset the I.C.

Connection Diagram (Pin Outs)

	Pin		Pin	
CARD PRESENT	1		16	DATA
RESET	2		15	STROBE
OSC-IN	3		14	+V
OSC-OUT	4	DIGITAL / ANALOG	13	HEAD IN 1
GND	5		12	HEAD IN 2
F/2F-OUT	6		11	GAIN SET
BIAS	7		10	SUM
REF	8		9	DRIVE

Recommended Circuit

This circuit is intended for use in systems employing F/2F data such as ID cards that conform to ISO 7811-2 or 7811-6.
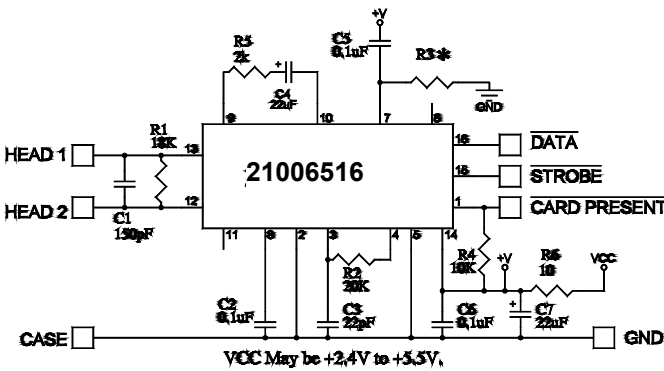
Tolerances: Resistors ±5%; C1, C3 ±5% NPO; other capacitors non-critical.

* R3 has different values for Rev B and Rev G. The table bellow shows the value of R3.

	Rev B	Rev G
R3	470K	1.5M

Table 2: Value of R3.

## Printed Circuit Board Layout Requirements

The I.C. is a combined digital and analog system. The analog signal pins are very low level. Good layout practice requires that there be a separation of head and other analog signals from the digital outputs. The digital signals are: DATA, STROBE, CARD PRESENT, F/2F OUT, OSC-OUT and OSC-IN. The analog signals in order of sensitivity are HEAD in 1&2, SUM, DRIVE, GSR and BIAS. The digital signals must not pass near the first four analog signals. The layout below illustrates the requirements.
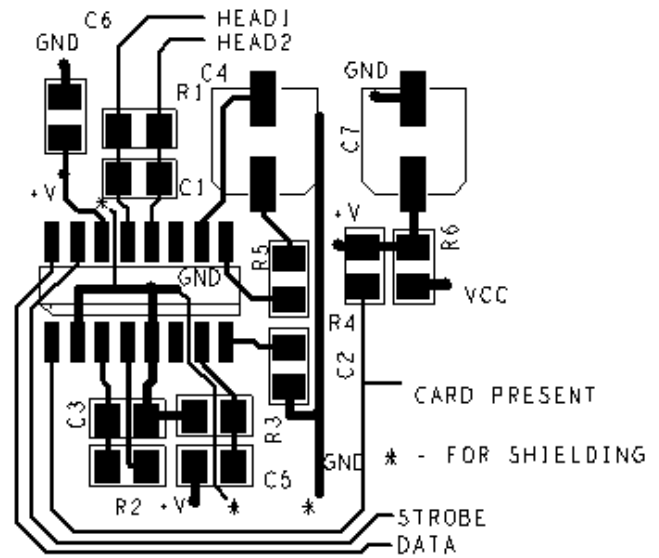
Caution

Keep Data, Strobe, and Card Present signals away from Head 1 and Head 2 signals.

SOIC Physical Dimensions
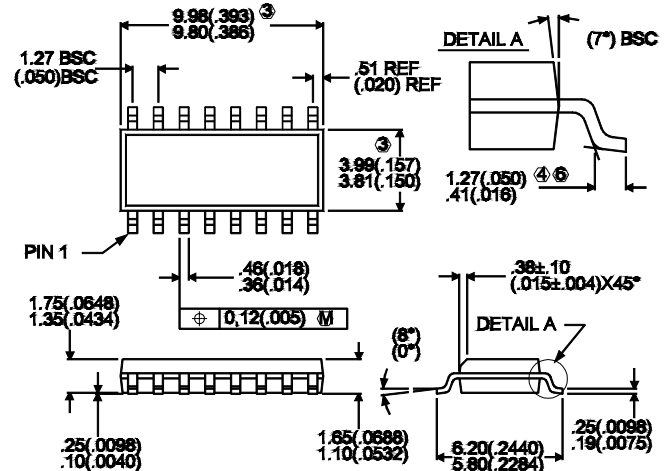
Notes: Unless otherwise specified
1. Dimensions in mm (in.)
2. Dimension and tolerancing per ANSI Y14.5m-1982
3. Reference Datum (Mold flash not included).
4. Length of terminal for soldering.
5. Flammability rating UL 94V-0
6. Thermal resistance JA=225, JC=190

MAGTEK