MC3471

FLOPPY DISK WRITE CONTROLLER (WITH ERASE DELAY)

SILICON MONOLITHIC INTEGRATED CIRCUIT

FLOPPY DISK WRITE CONTROLLER/HEAD DRIVER

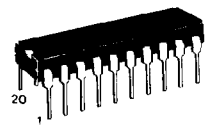
The MC3471 is a monolithic integrated Write Controller/Head Driver designed to provide the entire interface between the write data and head control signals and the heads (write and erase) for either Tunnel or straddle-erase floppy disk systems.

Provisions are made for selecting a range of accurately controlled write currents and for head selection during both read and write operation. Additionally, provisions are included for externally adjusting degauss period, inner/outer track compensation, and the delay from write gate to erase turn-on and turn-off.

Erase Delays are controlled by driving the delay inputs D1 and D2 with standard TTL open-collector logic (microprocessor compatible) or by using the external RC mode in which case the delay is one τ (K factor = 1.0).

In addition, an $\overline{\text{Inhibit}}$ output is provided which indicates that the heads are active during write, degauss, or erase.

- Head Selection — Current Steering Through Write Head and Erase Coil in Write Mode
- Adjustable On-Chip Delay of Erase Timing — Stable K Factor
- Delay Pins Logic Compatible for Direct Microprocessor Compatibility
- $\overline{\text{Inhibit}}$ Output Provided to Disable Read or Step During Head Active Time
- Provides High Impedance (Read Data Enable) During Read Mode
- Head Current (Write) Guaranteed ±3% (3.0 mA using R_{ext} = 10 kΩ)
- IRW Select Input Provides for Inner/Outer Track Compensation
- Degauss Period Externally Adjustable
- Specified With Head Supply (V_{BB}) from 10.8 V to 26.4 V
- Minimizes External Components
- See Application Note AN917 for Further Information



P SUFFIX
PLASTIC PACKAGE
CASE 738

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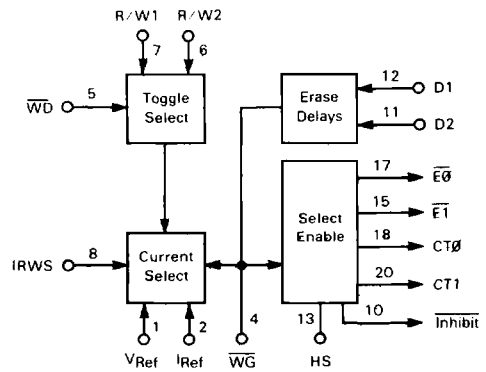
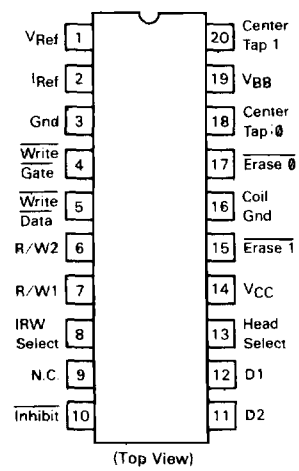
BLOCK DIAGRAM



PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 14)	V_{CC}	7.0	Vdc
Power Supply Voltage (Pin 19)	V_{BB}	30	Vdc
Input Voltage (Pins 4, 5, 8, 13)	V_I	5.75	Vdc
Output Applied Voltage (Pin 10)	V_O	7.0	Vdc
Open-Collector Sink Current (Pin 10)	I_O	25	mA
Storage Temperature	T_{stg}	-55 to +150	°C
Operating Junction Temperature	T_J	150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 14)	V_{CC}	+4.75 to +5.25	Vdc
Power Supply Voltage (Pin 19)	V_{BB}	+10.8 to +26.4	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25 V, V_{BB} = 10.8 to 26.4 V unless otherwise noted. Typicals given for V_{CC} = 5.0 V, V_{BB} = 12 V and T_A = 25°C unless otherwise noted.)

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Characteristics	Pins	Symbol	Min	Typ	Max	Unit
DIGITAL INPUT VOLTAGES						
Power Supply Current — V_{CC} V_{BB}		I_{CC} I_{BB}	— —	22 15	60 30	mA
High Level Input Voltage (V_{CC} = 4.75 V)	4, 8, 13	V_{IH}	2.0	—	—	V
Low Level Input Voltage (V_{CC} = 5.25 V)	4, 8, 13	V_{IL}	—	—	0.8	V
Input Clamp Voltage (I_{IK} = -12 mA)	4, 5, 8, 13	V_{IK}	—	-0.87	-1.5	V
Positive Threshold (V_{CC} = 5.0)	5	$V_{T(+)}$	1.5	1.75	2.0	V
Negative Threshold (V_{CC} = 5.0)	5	$V_{T(-)}$	0.7	0.98	1.3	V
Hysteresis ($V_{T(+)} - V_{T(-)}$) T_A = 0°C to +70°C T_A = 25°C	5	V_{HTS}	 0.2 0.4	 — 0.76	 — —	V
DIGITAL INPUT CURRENTS						
High Level Input Current (V_{CC} = 5.25 V, V_{BB} = 26.4 V, V_I = 2.4 V)	4, 5, 8, 13	I_{IH}	—	0.1	40	μA
Low Level Input Current (V_{CC} = 5.25 V, V_{BB} = 26.4 V, T_A = 25°C unless noted below) V_{BB} = 12 V V_{BB} = 24 V V_{CC} = 5.0 V V_{CC} = 5.0 V	4, 5, 8, 13 4 4 5 8, 13	I_{IL}	 — — — —	 — 0.36 0.76 0.46 0.39	 -1.6 — — — —	mA

ELECTRICAL CHARACTERISTICS (continued) (T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25 V, V_{BB} = 10.8 to 26.4 V unless otherwise noted. Typicals given for V_{CC} = 5.0 V, V_{BB} = 12 V and T_A = 25°C unless otherwise noted.)

Characteristics	Pins	Symbol	Min	Typ	Max	Unit
CENTER-TAP and ERASE OUTPUTS						
Output High Voltage (See Figure 14) (I_{OH} = −100 mA, V_{CC} = 4.75 V) V_{BB} = 10.8 to 26.4 V	18, 20	V_{OH}	V_{BB}-1.5	V_{BB}-1.0	—	V
Output Low Voltage (See Figure 14) (I_{OL} = 1.0 mA) V_{BB} = 12 V V_{BB} = 24 V	18, 20	V_{OL}	 —	 70	 150	mV
			—	70	150	
Output High Leakage Current (V_{OH} = 24 V, V_{CC} = 4.75 V, V_{BB} = 24 V)	15, 17	I_{OH}	—	0.01	100	μA
Output Low Voltage (See Figure 15) (I_{OL} = 90 mA, V_{CC} = 4.75 V) V_{BB} = 12 V V_{BB} = 24 V	15, 17	V_{OL}	 —	 0.27 0.27	 0.60 0.60	V
DIGITAL OUTPUT LEVEL ($\overline{\text{Inhibit}}$)						
High Level Output Current (V_{OH} = 7.0 V, V_{CC} = 4.75 V)	10	I_{OH}	—	—	100	μA
Low Level Output Voltage (I_{OL} = 4.0 mA, V_{CC} = 4.75 V)	10	V_{OL}	—	—	0.5	V
CURRENT SOURCE						
Reference Voltage	1	V_{Ref}	–	5.7	—	V
Degauss Voltage (See Text) (Voltage Pin 1 - Voltage Pin 2)	1	V_{DEG}	–	1.0	—	V
Bias Voltage	2	V_F	–	0.7	—	V
Write Current Off Leakage (V_{OH} = 30 V)	6, 7	I_{OH}	–	0.03	15	μA
Saturation Voltage (V_{BB} = 12 V)	6, 7	V_{sat}	—	0.85	2.7	V
Current Sink Compliance (For $V_{6, 7}$ = 4.0 V to 24 V, $V_{\overline{WG}}$ = 0.8 V)	6, 7	$\Delta I_{RW2, 1}$	—	15	40	μA
Average Value Write Current $\left(\frac{I_{Pin\ 6} + I_{Pin\ 7}}{2}\right)$ for V_{BB} = 10.8 to 26.4 V)	6, 7					
@ $I_{R/W} = I_{LOW}$, R = 10 k		$I_{\overline{R/W}(L)}$				mA
T_A = 25°C			2.91	3.0	3.09	
T_A = 0 to +70°C			2.84	—	3.16	
@ $I_{R/W} = I_{LOW}$, R = 5.0 k						
T_A = 25°C			5.64	5.89	6.14	
T_A = 0 to +70°C			5.51	—	6.28	
@ $I_{R/W} = I_{HI}$, R = 10 k ($I_{HI} = I_{LOW}$ + % I_{LOW})		$\Delta I_{\overline{R/W}(H)}$				%
T_A = 25°C			31.3	33.3	35.5	
T_A = 0 to +70°C			30.3	33.3	36.6	
Difference in Write Current ($\lvert I_{Pin\ 6} - I_{Pin\ 7} \rvert$ @ $I_{R/W} = I_{LOW}$, V_{BB} = 10.8 V to 26.4 V) R = 10 k	6, 7	$I_{R/W\Delta}$				mA
T_A = 25°C			—	0.003	0.015	
T_A = 0 to +70°C			—	—	0.023	
R = 5.0 k						
T_A = 25°C			—	—	0.030	
T_A = 0 to +70°C			—	—	0.046	

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ERASE DELAY ACCURACY (V_{CC} = 4.75 to 5.25 V, T_A = 0 to +70°C, V_{BB} = 10.8 to 26.4 V, — refer to Figure 9.)

Characteristics	Test	Min	Typ	Max	Unit
Delay Error, Pin 11, 12 D1, D2 = RC $\pm E_{D1,2}$, 30 kΩ ≤ R ≤ 300 kΩ	$E_{D1,2}$	—	—	15	%

AC SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C, V_{BB} = 24 V, I_{RWS} = 0.4 and $I_{R/W}$ = 3.0 mA unless otherwise noted.)

Characteristics (Note 1)	f_{in} (Note 2)	Min	Typ	Max	Unit
1. Delay from Head Select going low through 0.8 V to CTØ going high through 20 V.	HS, Pin 13	—	1.6	4.0	µs
2. Delay from Head Select going low through 0.8 V to CT1 going low through 1.0 V.	HS, Pin 13	—	2.1	4.0	µs
3. Delay from Head Select going high through 2.0 V to CTØ going low through 1.0 V.	HS, Pin 13	—	1.7	4.0	µs
4. Delay from Head Select going high through 2.0 V to CT1 going high through 20 V.	HS, Pin 13	—	1.4	4.0	µs
5. Delay from $\overline{WG}$ going low through 0.8 V to CT0 going low through 1.0 V.	$\overline{WG}$, Pin 4	—	1.3	4.0	µs
6. Delay from $\overline{WG}$ going low through 0.8 V to CT1 going high through 20 V.	$\overline{WG}$, Pin 4	—	0.8	4.0	µs
7. Delay from $\overline{WG}$ going low through 0.8 V to CT0 going high through 20 V.	$\overline{WG}$, Pin 4	-	0.75	4.0	µs
8. Delay from $\overline{WG}$ going low through 0.8 V to CT1 going low through 1.0 V.	$\overline{WG}$, Pin 4	-	1.2	4.0	µs
9. After $\overline{WG}$ goes high, delay from R/W1 turning off through 10% to CTØ going high through 20 V.	$\overline{WG}$, Pin 4	20	750	—	ns
10. After $\overline{WG}$ goes high, delay from R/W1 turning off through 10% to CT1 going low through 1.0 V.	$\overline{WG}$, Pin 4	20	1200	—	ns
11. After $\overline{WG}$ goes high, delay from R/W2 turning off through 10% to CTØ going low through 1.0 V.	$\overline{WG}$, Pin 4	20	1200	—	ns
12. After $\overline{WG}$ goes high, delay from R/W2 turning off through 10% to CT1 going high through 20 V.	$\overline{WG}$, Pin 4	20	600	—	ns
13. After $\overline{WG}$ goes low, delay from CTØ going low through 1.0 V to R/W1 turning on through 10%.	$\overline{WG}$, Pin 4	20	750	—	ns
14. After $\overline{WG}$ goes low, delay from CT1 going low through 1.0 V to R/W2 turning on through 10%.	$\overline{WG}$, Pin 4	20	750	—	ns
15. After $\overline{WG}$ goes low, fall time (10% to 90%) of R/W1.	$\overline{WG}$, Pin 4	—	5.0	200	ns
16. After $\overline{WG}$ goes low, fall time (10% to 90%) of R/W2.	$\overline{WG}$, Pin 4	—	5.0	200	ns
17. Setup time, Head Select going low before $\overline{WG}$ going low.	$\overline{WG}$, Pin 4	4.0	—	—	µs
18. $\overline{\text{Write Data}}$ low Hold Time	$\overline{WD}$, Pin 5	200	—	—	ns
19. $\overline{\text{Write Data}}$ high Hold Time	$\overline{WD}$, Pin 5	500	—	—	ns
20. Delay from $\overline{WG}$ going high through 2.0 V to R/W 1 turning off through 10% of on value.	$\overline{WG}$, Pin 4	—	3.9	—	µs
21. Delay from $\overline{WG}$ going low thru 0.8 V to $\overline{\text{Inhibit}}$ going low thru 0.5 V	$\overline{WG}$, Pin 4	—	0.08	4.0	µs
22. After $\overline{WG}$ goes high, delay from R/W1 turning off thru 10% to $\overline{\text{Inhibit}}$ going high thru 1.5 V (10 k pullup on Inhibit, Note 3)	$\overline{WG}$, Pin 4	20	750	—	ns
23. After $\overline{WG}$ goes high, delay from $\overline{E1}$ going high thru 23 V to $\overline{\text{Inhibit}}$ going high thru 1.5 V (10 k pullup on Inhibit, Note 3)	$\overline{WG}$	20	750	—	ns

Notes:
1. Test numbers refer to encircled numbers in Figures 3 & 16.
2. AC test waveforms applied to the designated pins as follows:

Pin	f_{in}	Amplitude	Duty Cycle
HS, Pin 13	50 kHz	0.4 to 2.4 V	50%
$\overline{WG}$, Pin 4	50 kHz	0.4 to 2.4 V	50%
$\overline{WD}$, Pin 5	1.0 MHz	0.2 to 2.4 V	50%

3. Test Conditions 22, or 23, whichever produces the longer delay, will control Inhibit.

AC SWITCHING CHARACTERISTICS (continued)
(V_{CC} = 5.0 V, T_A = 25°C, V_{BB} = 24 V, $\overline{WG}$ = 0.4 unless otherwise noted)

Characteristics (Note 4)	Min	Typ	Max	Unit
1. Delay from $\overline{\text{Write Data}}$ going low through 0.9 V to R/W1 turning on through 50%.	—	85	—	ns
2. Delay skew, difference of R/W1 turning off and R/W2 turning on through 50% after $\overline{\text{Write Data}}$ going low through 0.9 V.	—	1.0	±40	ns
3. Delay from $\overline{\text{Write Data}}$ going low through 0.9 V to R/W1 turning off through 50%.	—	80	—	ns
4. Delay skew, difference of R/W1 turning on and R/W2 turning off 50% after $\overline{\text{Write Data}}$ going low through 0.9 V.	—	1.0	±40	ns
5. Fall time, 10% to 90%, of R/W1	—	1.7	200	ns
6. Fall time, 10% to 90%, of R/W2	—	1.7	200	ns
7. Rise time, 90% to 10%, of R/W1	—	12	200	ns
8. Rise time, 90% to 10%, of R/W2	—	12	200	ns

Note 4. Test numbers refer to encircled numbers in Figures 2 & 15.
f_{in} = 1.0 MHz, 50% Duty Cycle and Amplitude of 0.2 V to 2.4 V.

PIN DESCRIPTION TABLE

Name	Symbol	Pin	Description
Head Select	HS	13	Head Select input selects between the head I/O pins; center-tap, erase, and read/write. A HIGH selects Head 0 and a LOW selects Head 1.
$\overline{\text{Write Gate}}$	$\overline{WG}$	4	$\overline{\text{Write Gate}}$ input selects the mode of operation. HIGH selects the read mode, while LOW selects the Write Control mode and forces the write current.
$\overline{\text{Write Data}}$	$\overline{WD}$	5	$\overline{\text{Write Data}}$ input controls the turn on/off of the write current. The internal divide-by-two flip-flop toggles on the negative going edge of this input to direct the current alternately to the two halves of the head coils.
IRW Select	IRWS	8	IRW Select input selects the amount of write current to be used. When LOW, the current equals the value found in Figure 5, according to the external resistor. When HIGH, the current equals the low current + 33%.
V_{Ref} I_{Ref}	V_{Ref} I_{Ref}	1 2	A resistor between these pins sets the write current. (Refer to Figure 4.) A capacitor from V_{Ref} to Gnd will adjust the Degauss period.
Center-Tap 0	CT0	18	Center-Tap 0 output is connected to the center tap of Head 0. It will be pulled to Gnd or V_{BB} (+12 or +24) depending on mode and head selection.
$\overline{\text{Erase 0}}$	$\overline{E0}$	17	$\overline{\text{Erase 0}}$ will be LOW for writing on Head 0, and floating for other conditions.
Center-Tap 1	CT1	20	Center-Tap 1 output is connected to the center tap of Head 1. It will be pulled to Gnd or V_{BB} (+12 or +24) depending on mode and head selection.
$\overline{\text{Erase 1}}$	$\overline{E1}$	15	$\overline{\text{Erase 1}}$ will be LOW for writing on Head 1, and floating for other conditions.
R/W2	R/W2	6	R/W2 input is one of the differential inputs that sinks current during writing, being the opposite phase of R/W1. It will be connected to one side of the heads.
R/W1	R/W1	7	R/W1 input is one of the differential inputs that sinks current during writing, being the opposite phase of R/W2. It will be connected to one side of the heads.
	V_{CC}	14	+5.0 V Power
	V_{BB}	19	+12 V or + 24 V Power
	Gnd	16	Coil grounds
	Gnd	3	Reference and logic ground
Delay 1	D1	12	Erase Turn-On Delay adjust (RC or Logic)
Delay 2	D2	11	Erase Turn-Off Delay adjust (RC or Logic)
Inhibit	$\overline{\text{Inhibit}}$	10	Active low open-collector output provided to indicate heads are active in the write, degauss or erase mode. (Used for step or read inhibit.)

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FIGURE 1 — LOGIC DIAGRAM

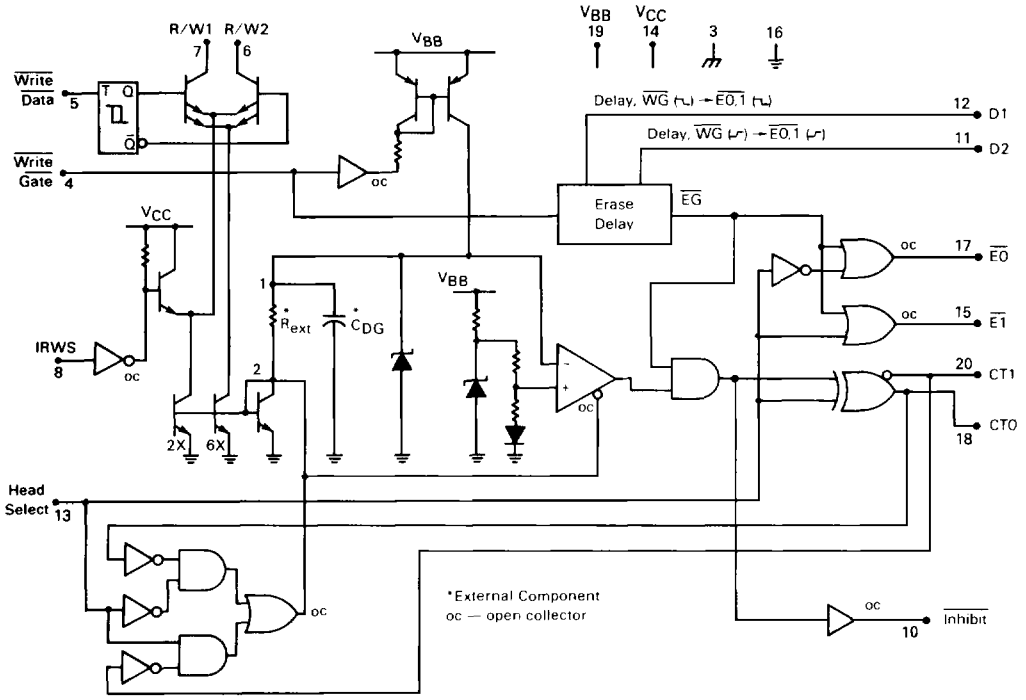


FIGURE 2 — R/W1 AND R/W2 RELATIONSHIP

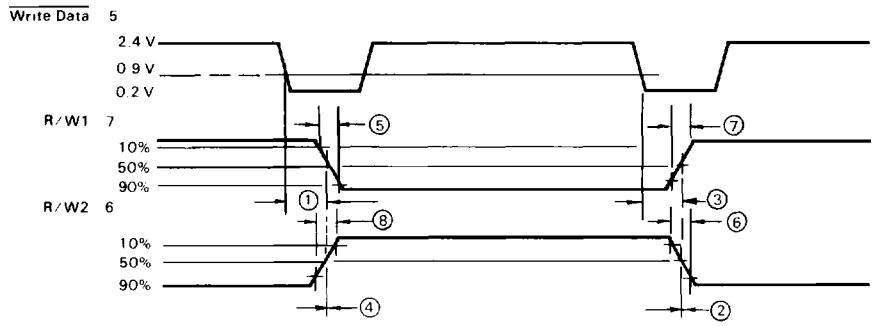


FIGURE 3 — AC TIMING DIAGRAM

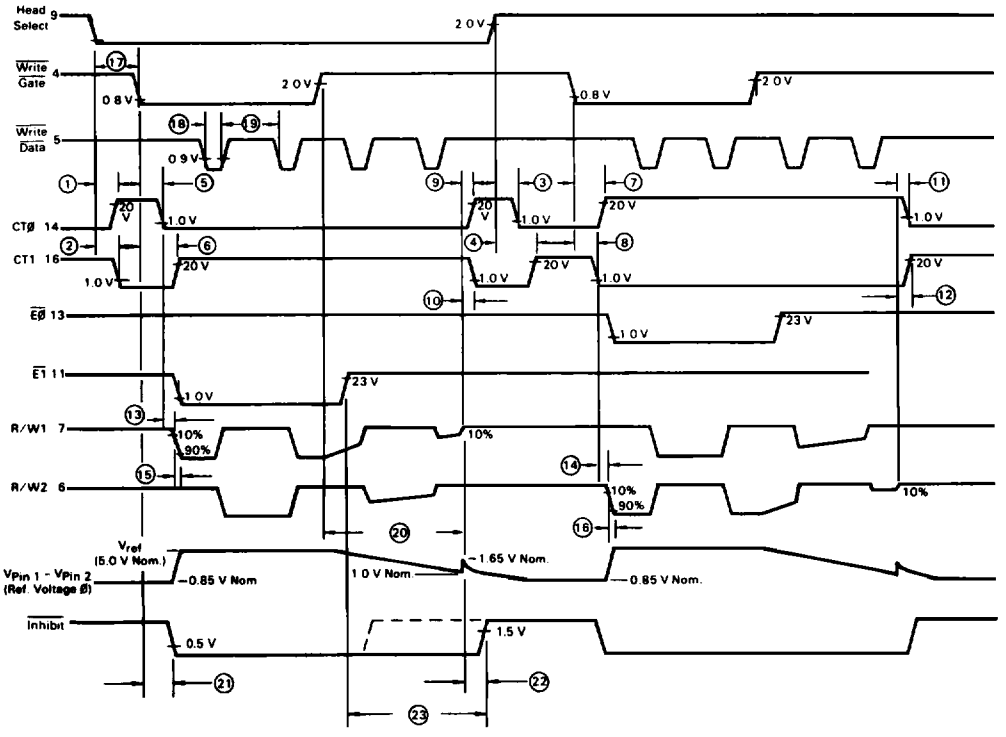
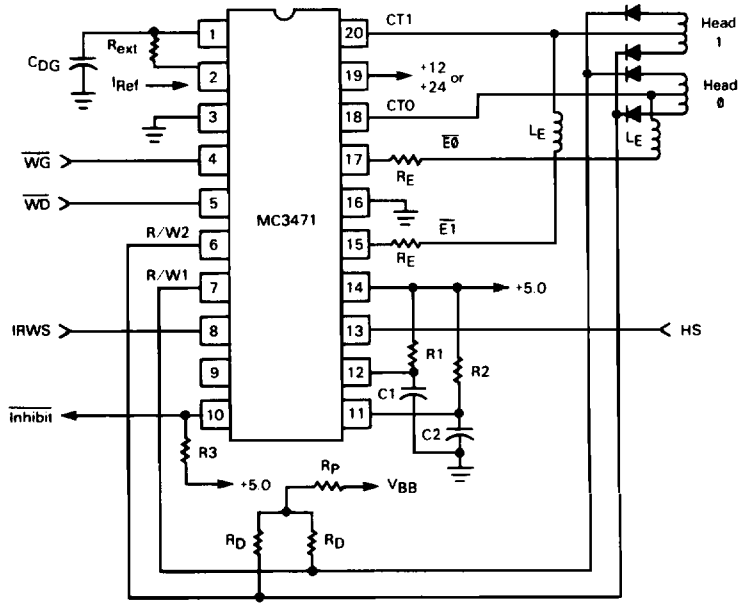


FIGURE 4 — TYPICAL APPLICATION



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APPLICATION INFORMATION

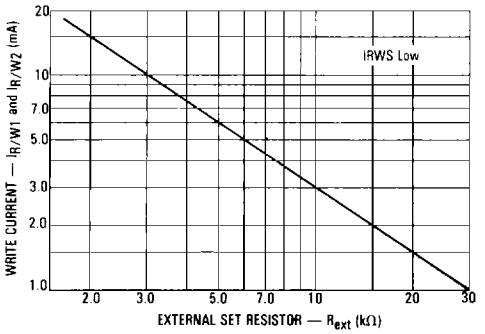
The MC3471P serves as a complete interface between the Write Control functional signals (Head Select, Write Data, Write Gate and inner track compensation, IRWS) and the head itself. A typical configuration is shown in Figure 4. L_E's are erase coils.

WRITE CURRENT SELECTION

Although the MC3471P has been specified for 3.0 mA write current (with a 10 kΩ external resistor), a range of write current values can be chosen by varying R_{ext} using the plot in Figure 5. This current can also be derived using the relationship $I_{Write}\ (mA) = \frac{30}{R_{ext}(k\Omega)}$

I_{Ref}, the current flowing in R_{ext} (required only for dissipation calculations) can be worst case using the fact that the differential voltage between Pins 1 and 2 (V_{Ref}) shown in Figure 3 never exceeds 5.0 volts. With a low value of R_{ext} = 1.0 kΩ, P_D = 25 mW.

FIGURE 5 — WRITE CURRENT versus R_{ext}



WRITE CURRENT DAMPING

Referring to Figure 4, resistors R_D are used to dampen any ringing that results from applying the relatively fast risetime write current pulse to the inductive head load. Values chosen will be a funciton of head characteristics and the desired damping. R_P serves as a common pullup resistor to the head supply V_{BB}.

DEGAUSS PERIOD

Degauss of the read/write head can be accomplished at the end of each write operation by attaching a capacitor from Pin 1 to ground. The time relationship that results is shown in Figure 7. A simplified diagram of this function is shown in Figure 6.

While $\overline{WG}$ is low, the selected write current flows into Pin 6 or Pin 7 (R/W1 or R/W2) and is mirrored through the external resistor, R_{ext}. The degauss capacitor, C_{DG}, will be charged to approximately 5.7 volts. After $\overline{WG}$ goes high, the voltage on C_{DG} begins to decay toward 0.7 V. When the voltage reaches the comparator threshold of 1.7 V, the comparator output triggers the internal logic to completely turn off the write current. At this point, the pulse amplitude on the R/W1 and R/W2 pins has returned to 10% of its maximum value.

Figure 7, Degauss Period shows the relationship between C_{DG} and Degauss Period for R_{ext} = 10 kΩ. This period is equal to the exponential delay time for the voltage as mentioned plus internal delay times.

FIGURE 6 — SIMPLIFIED DEGAUSS CIRCUIT

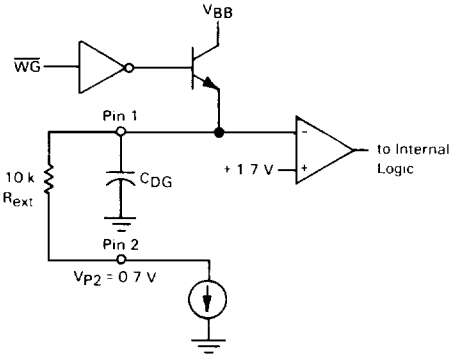
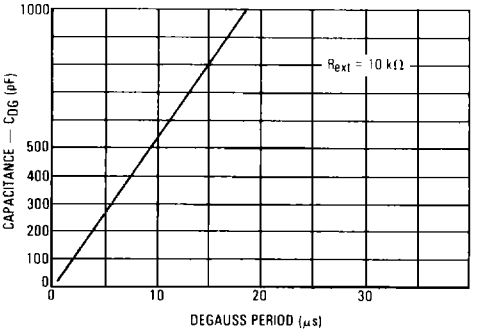


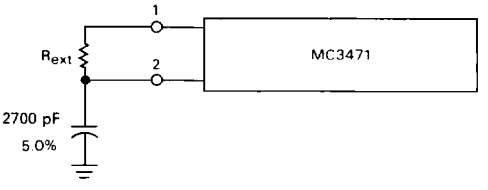
FIGURE 7 — DEGAUSS PERIOD versus CAPACITANCE (C_{DG})



POWER-UP WRITE CURRENT CONTROL

During power-up, under certain conditions (V_{BB} comes up first while $\overline{WG}$ is low), there can be a write current transient on Pins 6 and 7 (R/W1 and R/W2) of sufficient magnitude to cause writing to occur if the head is loaded.

This transient can be eliminated by placing a capacitor from Pin 2 to ground. This also delays the write current when $\overline{WG}$ goes low and this delay must be accounted for when the capacitor on Pin 2 is used. The delay is 3.0 μs for a 2700 pF capacitor, and R_{ext} = 10 kΩ. Values up to 7000 pF may be used.



See Application Note AN917 for further information.

ERASE DELAY

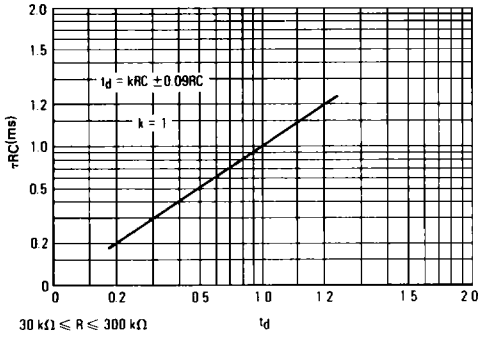
The MC3471P can be used with both straddle and tunnel erase heads. When using the tunnel erase heads, it is necessary to delay the erase current in time with respect to $\overline{WG}$ due to the physical placement of the erase gap behind the R/W gap on the heads. The amount of delay required depends upon the disk rotation velocity, recording density and format. Turn-on delay and turn-off delay must also be independent to guarantee erase is on for the entire block.

Nominal delays of 500 μs turn-on; and 1.0 ms turn-off are available by adjusting the value of R1, R2 and C1, C2 shown in Figure 4. These delays are adjustable over a broad range as shown in Figure 9 to achieve any practical delay required. By using 5% capacitors and 1% resistors, total timing accuracy is better than ±15% over temperature and supply. Timing is shown in Figure 10.

In applications using logic or microprocessor controlled delays, the D1 and D2 inputs can be used directly to turn-on and turn-off the erase current. (Controlling outputs should be Open-collector w/10 k pullup). Figure 11 shows the relative timing involved for the microprocessor and logic controlled applications.

In straddle erase systems, the erase delays can be eliminated by pulling D1 and D2 high thru a 10 kΩ pullup resistor to +5.0 V.

FIGURE 9 — TYPICAL $\overline{WG}$ TO EØ, 1 DELAY versus RC



ERASE CURRENT

The value of R_E, the erase current set resistor, is found by referring to Figure 12 and selecting the desired erase current.

Looking at the simplified erase current path in Figure 12, when writing, CTØ will be high ($V_{OH(min)}$ = 22.5 V) and EØ will be low ($V_{OL(max)}$ = 0.6 V). If the erase coil resistance is 10 Ω and 40 mA of erase current is desired then:

$$(R_E + 10\ \Omega) \times 40\ mA = (22.5 - 0.6)\ V$$

or

$$R_E = \frac{21.9\ V}{0.04\ A} - 10\ \Omega = 537\ \Omega$$

$$P_D = (537)\ (0.04)^2 = 0.86\ W$$

This gives the minimum value R_E for worst case V_{OH}/V_{OL} conditions. It is also recommended that a diode be used as indicated for inductive back emf suppression.

FIGURE 10 — DELAY INPUT FUNCTION/TIMING WITH RC ELEMENTS

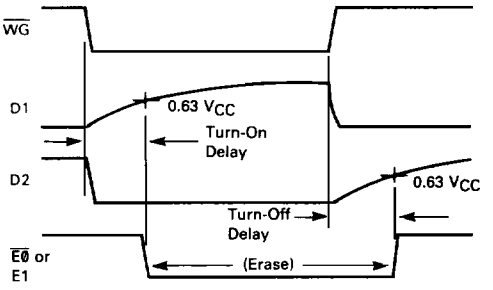


FIGURE 11 — DELAY INPUT FUNCTION/TIMING WITH LOGIC CONTROL

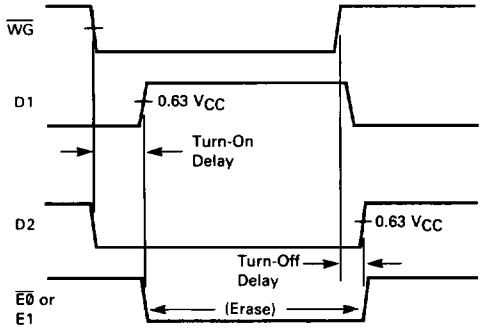


FIGURE 12 — ERASE CURRENT (R_E Selection)

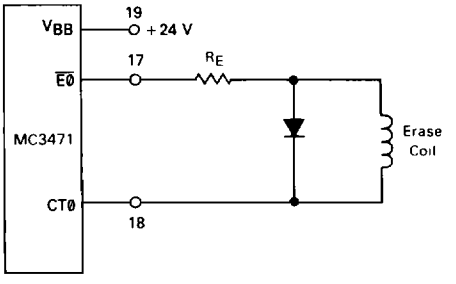
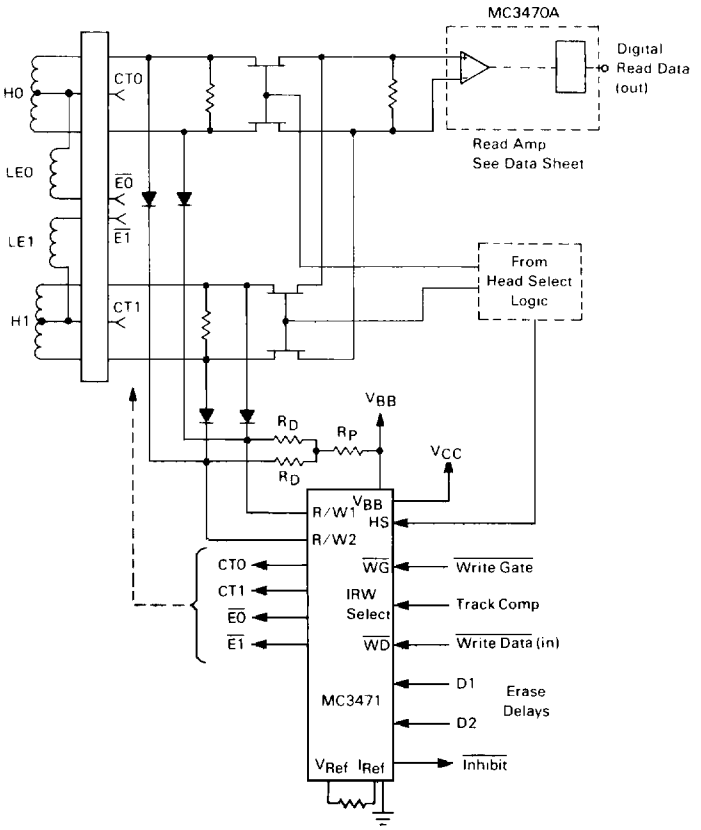


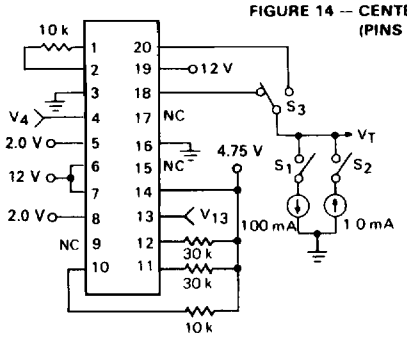
FIGURE 13 — TYPICAL DUAL HEAD FLOPPY DISK SYSTEM USING FET GATE READ CHANNEL SELECTION AND MC3471/MC3470A



Function	CT0	CT1	E0	E1
Write 0	V_{BB}	0 V	On	Off
Write 1	0 V	V_{BB}	Off	On
Read 0	0 V	V_{BB}	Off	Off
Read 1	V_{BB}	0 V	Off	Off

TEST FIGURES

FIGURE 14 — CENTER TAP OUTPUT VOLTAGE (PINS 18 AND 20)

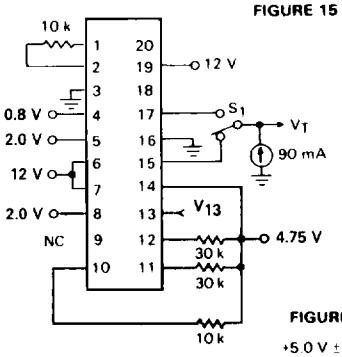


CONDITIONS

Measure V_T	S_1	S_2	S_3	V_4*	V_{13}*
V_{OH} (P18)	On	Off	P 18	0.8	2.0
				2.0	0.8
V_{OH} (P20)	On	Off	P 20	2.0	2.0
				0.8	0.8
V_{OL} (P18)	Off	On	P 18	0.8	0.8
				2.0	2.0
V_{OL} (P20)	Off	On	P 20	2.0	0.8
				0.8	2.0

*Volts

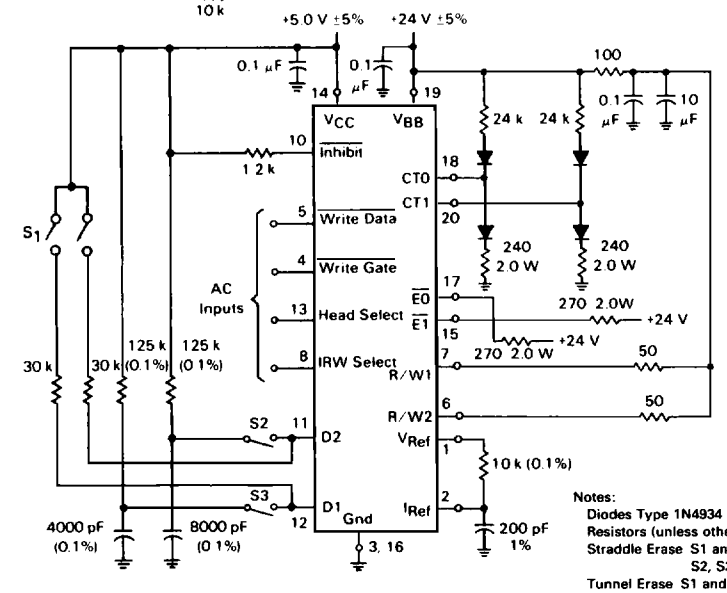
FIGURE 15 — ERASE OUTPUT LOW VOLTAGE (PINS 15 AND 17)



CONDITIONS

Measure V_T	Set S_1	Set V_{13}
V_{OL} (P15)	P15	0.8V
V_{OL} (P17)	P17	2.0 V

FIGURE 16 — TIMING TEST CIRCUIT



Notes:
Diodes Type 1N4934
Resistors (unless otherwise noted) are 1/4 W 5%
Straddle Erase S1 and S_4 Closed
S2, S3 Open
Tunnel Erase S1 and S_4 Open
S2, S3 Closed

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