CD4089B Types

CMOS

Binary Rate Multiplier

High-Voltage Types (20-Volt Rating)

■ CD4089B is a low-power 4-bit digital rate multiplier that provides an output pulse rate that is the clock-input-pulse rate multiplied by 1/16 times the binary input. For example, when the binary input number is 13, there will be 13 output pulses for every 16 input pulses. This device may be used in conjunction with an up/down counter and control logic used to perform arithmetic operations (adds, subtract, divide, raise to a power), solve algebraic and differential equations, generate natural logarithms and trigonometric functions, A/D and D/A conversions, and frequency division.

For words of more than 4 bits, CD4089B devices may be cascaded in two different modes: an Add mode and a Multiply mode (see Figs. 14 and 15). In the Add mode some of the gaps left by the more significant unit at the count of 15 are filled in by the less significant units. For example, when two units are cascaded in the Add mode and programmed to 11 and 13, respectively, the more significant unit will have 11 output pulses for every 16 input pulses and the other unit will have 13 output pulses for every 256 input pulses for a total of

$$\frac{11}{16} + \frac{13}{256} = \frac{189}{256}$$

In the Multiply mode the fraction programmed into the first rate multiplier is multiplied by the fraction programmed into the second multiplier. Thus the output rate will be

$$\frac{11}{16} \times \frac{13}{16} = \frac{143}{256}$$

Features:

■ Cascadable in multiples of 4-bits
■ Set to "15" input and "15" detect output
■ 100% tested for quiescent current at 20 V
■ 5-V, 10-V, and 15-V parametric ratings
■ Standardized, symmetrical output characteristics
■ Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
■ Noise margin (full package-temperature range) =

$$1 \text{ V at } V_{DD} = 5 \text{ V}$$
$$2 \text{ V at } V_{DD} = 10 \text{ V}$$
$$2.5 \text{ V at } V_{DD} = 15 \text{ V}$$

■ Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

■ Numerical control
■ Instrumentation
■ Digital filtering
■ Frequency synthesis

The CD4089B has an internal synchronous 4-bit counter which, together with one of the four binary input bits, produces pulse trains as shown in Fig. 2.

If more than one binary input bit is high, the resulting pulse train is a combination of the separate pulse trains as shown in Fig. 2.

The CD4089B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).
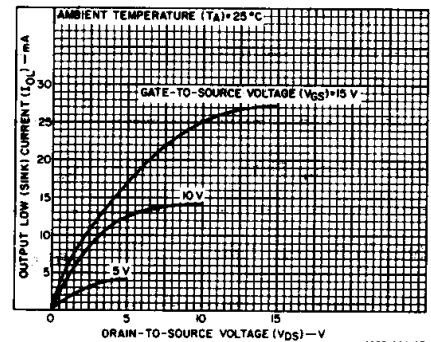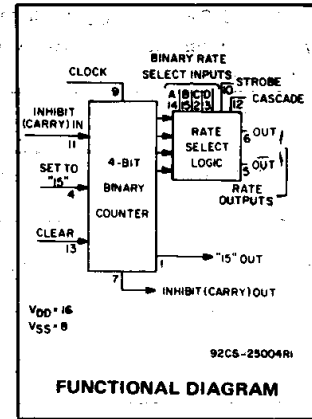

FUNCTIONAL DIAGRAM

Fig. 1 – Typical output low (sink) current characteristics.
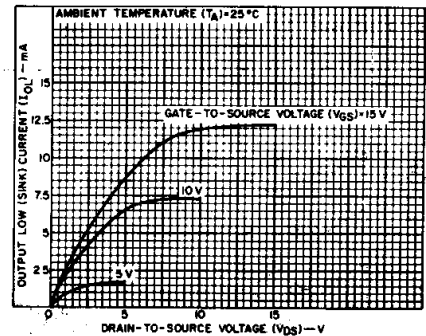

Fig. 2 - Minimum output low (sink) current characteristics.
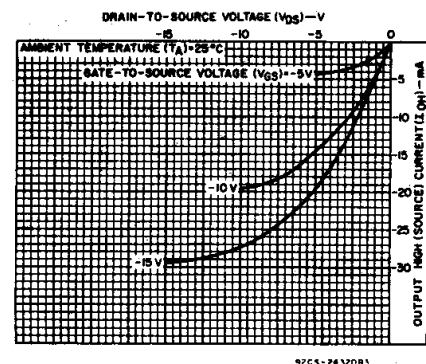
Fig. 3 – Typical output high (source) current characteristics.

3

COMMERCIAL CMOS
HIGH VOLTAGE ICs

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_DD)

Voltages referenced to V_SS Terminal) .... −0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS .... −0.5V to V_DD +0.5V

DC INPUT CURRENT, ANY ONE INPUT .... ±10mA

POWER DISSIPATION PER PACKAGE (P_D):

For T_A = −55°C to +100°C 500mW

For T_A = +100°C to +125°C... Derate Linearity at 12mW/°C to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW

OPERATING-TEMPERATURE RANGE (T_A).. −55°C to +125°C

STORAGE TEMPERATURE RANGE (T_stg)... −65°C to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max .... +265°C

RECOMMENDED OPERATING CONDITIONS at $T_A = 25°C$, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC		V_{DD} (V)	LIMITS		UNITS
			Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)			3	18	V
Set or Clear Pulse Width,	t_W	5	160	—	ns
		10	90	—	
		15	60	—	
Clock Pulse Width,	t_W	5	330	—	ns
		10	170	—	
		15	100	—	
Clock Frequency,	f_{CL}	5	dc	1.2	MHz
		10		2.5	
		15		3.5	
Clock Rise or Fall Time,	t_{rCL} or t_{fCL}	5, 10,15	—	15	μs
Inhibit In Setup Time,	t_{SU}	5	100	—	ns
		10	40	—	
		15	20	—	
Inhibit In Removal Time,	t_{REM}	5	240	—	ns
		10	130	—	
		15	110	—	
Set Removal Time,	t_{REM}	5	150	—	ns
		10	80	—	
		15	50	—	
Clear Removal Time,	t_{REM}	5	60	—	ns
		10	40	—	
		15	30	—	
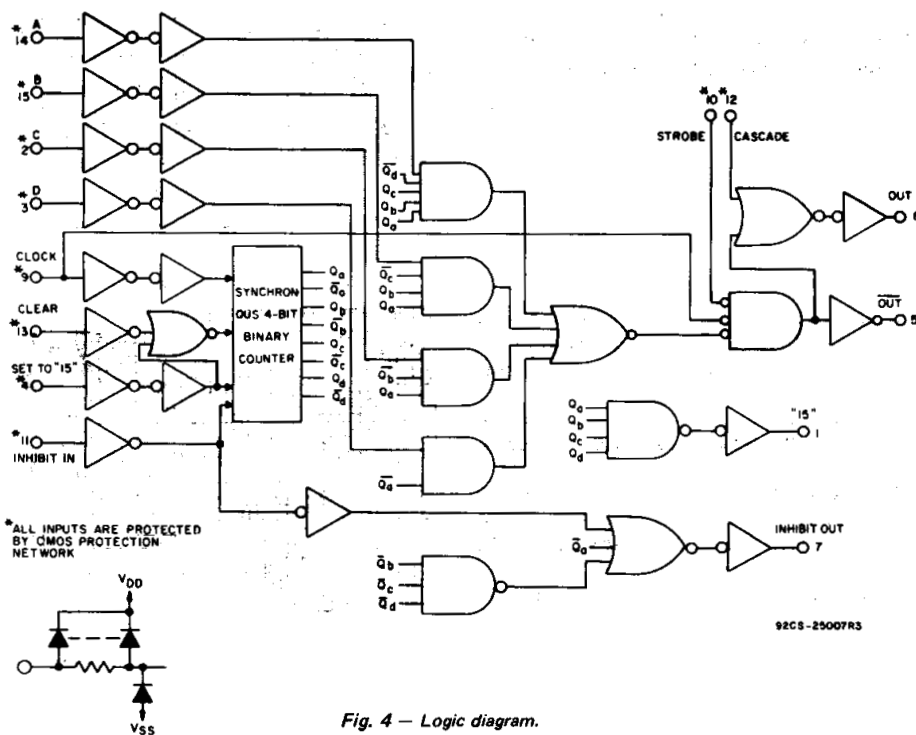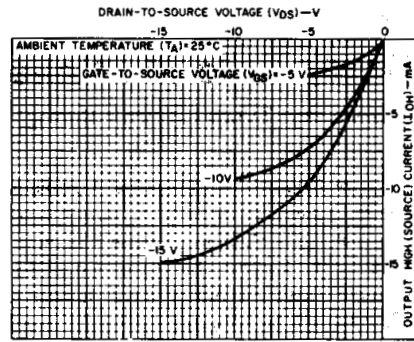
Fig. 5 — Minimum output high (source) current characteristics.
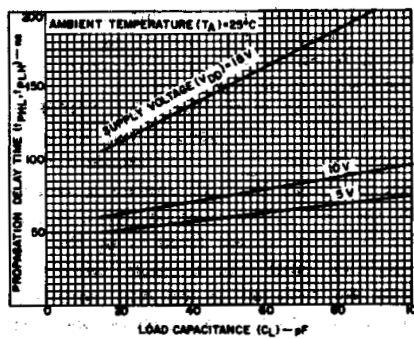

Fig. 6 — Typical propagation delay time as a function of load capacitance (Clock or Strobe to Out).
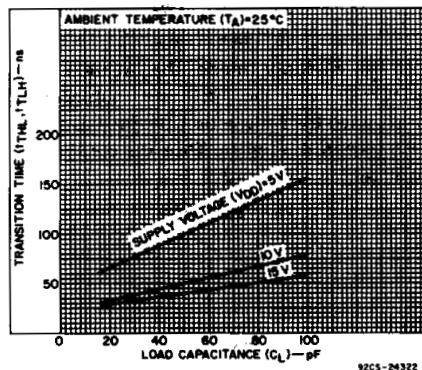

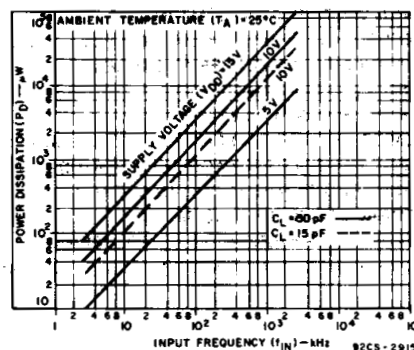Fig. 7 — Typical transition time as a function of load capacitance.

Fig. 8 — Typical dynamic power dissipation as a function of input frequency.

Fig. 4 — Logic diagram.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$;
Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} V	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Propagation Delay Time, t_{PHL}, t_{PLH} Clock to $\overline{Out}$	5	–	110	220	
	10	–	55	110	
	15	–	45	90	ns
Clock or Strobe to Out	5	–	150	300	
	10	–	75	150	
	15	–	60	120	
Clock to Inhibit Out High Level to Low Level	5	–	360	720	
	10	–	160	320	ns
	15	–	110	220	
Low Level to High Level	5	–	250	500	
	10	–	100	200	ns
	15	–	75	150	
Clear to Out	5	–	380	760	
	10	–	175	350	ns
	15	–	130	260	
Clock to "9" or "15" Out	5	–	300	600	
	10	–	125	250	ns
	15	–	90	180	
Cascade to Out	5	–	90	180	
	10	–	45	90	ns
	15	–	35	70	
Inhibit In to Inhibit Out	5	–	160	320	
	10	–	75	150	
	15	–	55	110	ns
Set to Out	5	–	330	660	
	10	–	150	300	
	15	–	110	220	
Transition Time, t_{THL}, t_{TLH}	5	–	100	200	
	10	–	50	100	ns
	15	–	40	80	
Maximum Clock Frequency, f_{CL}	5	1.2	2.4	–	
	10	2.5	5	–	MHz
	15	3.5	7	–	
Minimum Clock Pulse Width, t_W	5	–	165	330	
	10	–	85	170	ns
	15	–	50	100	
Clock Rise or Fall Time, t_{rCL}, t_{fCL}	5	–	–	15	
	10	–	–	15	μs
	15	–	–	15	
Minimum Set or Clear Pulse Width, t_W	5	–	80	160	
	10	–	45	90	ns
	15	–	30	60	
Minimum Inhibit-In Setup Time, t_{SU}	5	–	50	100	
	10	–	20	40	ns
	15	–	10	20	
Minimum Inhibit In Removal Time, t_{REM}	5	–	120	240	
	10	–	65	130	ns
	15	–	55	110	
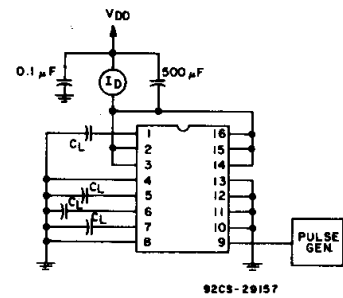
Fig. 9 — *Dynamic power dissipation test circuit.*
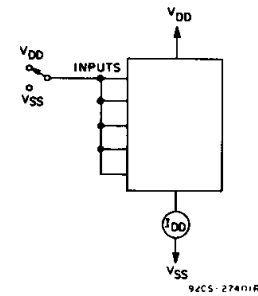
Fig. 10 — *Quiescent device current test circuit.*

NOTE
MEASURE INPUTS SEQUENTIALLY, TO BOTH V_{DD} AND V_{SS} CONNECT ALL UNUSED INPUTS TO EITHER V_{DD} OR V_{SS}.
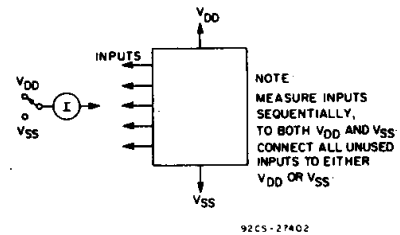
Fig. 11 — *Input-current test circuit.*

NOTE: TEST ANY COMBINATION OF INPUTS
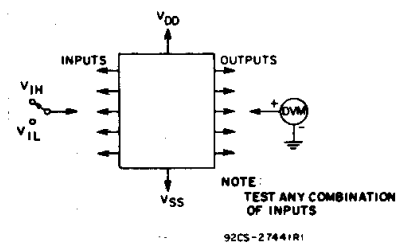
Fig. 12 — *Input-voltage test circuit.*

"15"OUT — 1	16 — V_{DD}
C — 2	15 — B
D — 3	14 — A
SET TO "15" — 4	13 — CLEAR
$\overline{OUT}$ — 5	12 — CASCADE
OUT — 6	11 — INHIBIT IN (CARRY)
INHIBIT OUT (CARRY) — 7	10 — STROBE
V_{SS} — 8	9 — CLOCK

92CS-25005R1
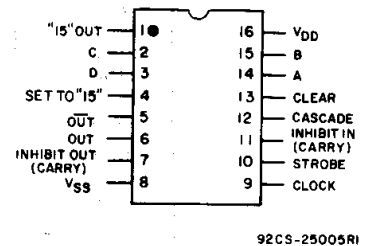
TOP VIEW

TERMINAL ASSIGNMENT

COMMERCIAL CMOS HIGH VOLTAGE ICs

3

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C (cont'd)
Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} V	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Minimum Set Removal Time, t_{REM}	5	—	75	150	ns
	10	—	40	80	
	15	—	25	50	
Minimum Clear Removal Time, t_{REM}	5	—	30	60	ns
	10	—	20	40	
	15	—	15	30	
Input Capacitance, C_{IN}	Any Input	—	5	7.5	pF

STATIC ELECTRICAL CHARACTERISTICS

CHARAC-TERISTIC	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD} Max.	—	0,5	5	5	5	150	150	—	0.04	5	μA
	—	0,10	10	10	10	300	300	—	0.04	10	
	—	0,15	15	20	20	600	600	—	0.04	20	
	—	0,20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	—	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	—	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	—	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	—	
Output Voltage: Low-Level, V_{OL} Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	—	0,5	5	4.95				4.95	5	—	
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage V_{IL} Max.	0.5,4.5	—	5	1.5				—	—	1.5	V
	1,9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	—	5	3.5				3.5	—	—	
	1,9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current I_{IN} Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	±10^{-5}	±0.1	μA

TRUTH TABLE

INPUTS										OUTPUTS			
Number of Pulses or Input Logic Level (0 = Low; 1 = High; X = Don't Care)										Number of Pulses or Output Logic Level (L = Low; H = High)			
D	C	B	A	CLK	INH IN	STR	CAS	CLR	SET	OUT	$\overline{OUT}$	INH OUT	"15" OUT
0	0	0	0	16	0	0	0	0	0	L	H	1	1
0	0	0	1	16	0	0	0	0	0	1	1	1	1
0	0	1	0	16	0	0	0	0	0	2	2	1	1
0	0	1	1	16	0	0	0	0	0	3	3	1	1
0	1	0	0	16	0	0	0	0	0	4	4	1	1
0	1	0	1	16	0	0	0	0	0	5	5	1	1
0	1	1	0	16	0	0	0	0	0	6	6	1	1
0	1	1	1	16	0	0	0	0	0	7	7	1	1
1	0	0	0	16	0	0	0	0	0	8	8	1	1
1	0	0	1	16	0	0	0	0	0	9	9	1	1
1	0	1	0	16	0	0	0	0	0	10	10	1	1
1	0	1	1	16	0	0	0	0	0	11	11	1	1
1	1	0	0	16	0	0	0	0	0	12	12	1	1
1	1	0	1	16	0	0	0	0	0	13	13	1	1
1	1	1	0	16	0	0	0	0	0	14	14	1	1
1	1	1	1	16	0	0	0	0	0	15	15	1	1
X	X	X	X	16	1	0	0	0	0	†	†	H	†
X	X	X	X	16	0	1	0	0	0	L	H	1	1
X	X	X	X	16	0	0	1	0	0	H	*	1	1
1	X	X	X	16	0	0	0	1	0	16	16	H	L
0	X	X	X	16	0	0	0	1	0	L	H	H	L
X	X	X	X	16	0	0	0	X	1	L	H	L	H

* Output same as the first 16 lines of this truth table (depending on values of A, B, C, D).
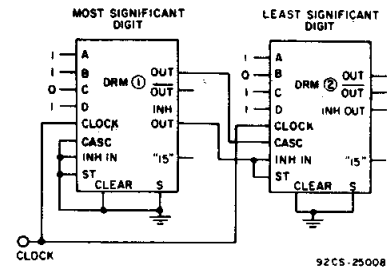† Depends on internal state of counter.

Fig. 13 – Two CD4089B's cascaded in the "Add" mode with a preset number of 189 $\left(\frac{11}{16} + \frac{13}{256} = \frac{189}{256}\right)$
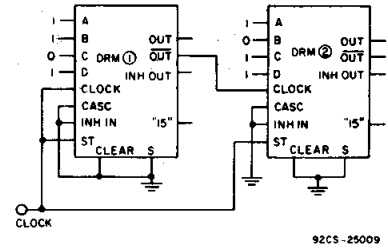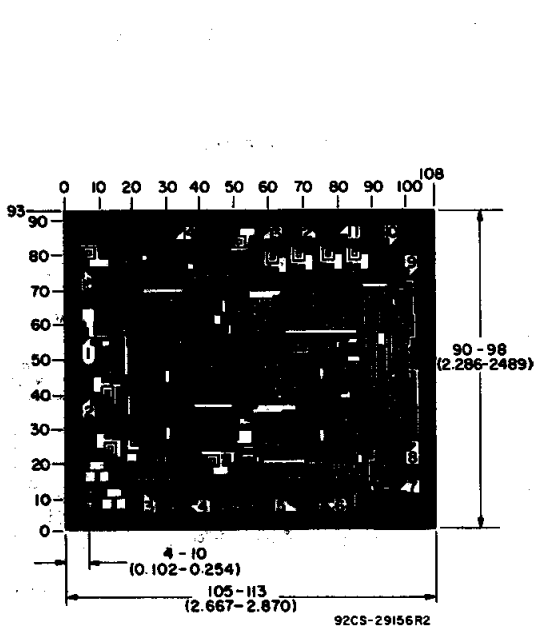

Fig. 14 – Two CD4089B's cascaded in the "Multiply" mode with a preset number of 143 $\left(\frac{11}{16} \times \frac{13}{16} = \frac{143}{256}\right)$.

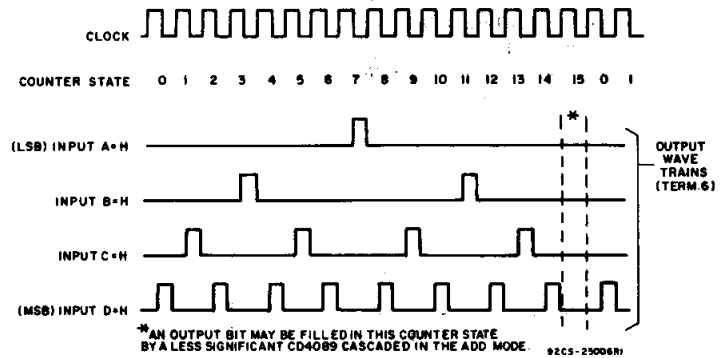
Dimensions and Pad Layout for CD4089BH

Fig. 15 – Timing diagram.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10⁻³ inch).

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
CD4089BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4089BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4089BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
CD4089BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4089BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4089BNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4089BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4089BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4089BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4089BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4089BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4089BNSR	SO	NS	16	2000	367.0	367.0	38.0
CD4089BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

DIM PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

1   7

0.065 (1,65)
0.045 (1,14)

C

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°-15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package is hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E.   Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R−PDIP−T**)

PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14) △D

0.045 (1,14) / 0.030 (0,76) △D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option △D

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

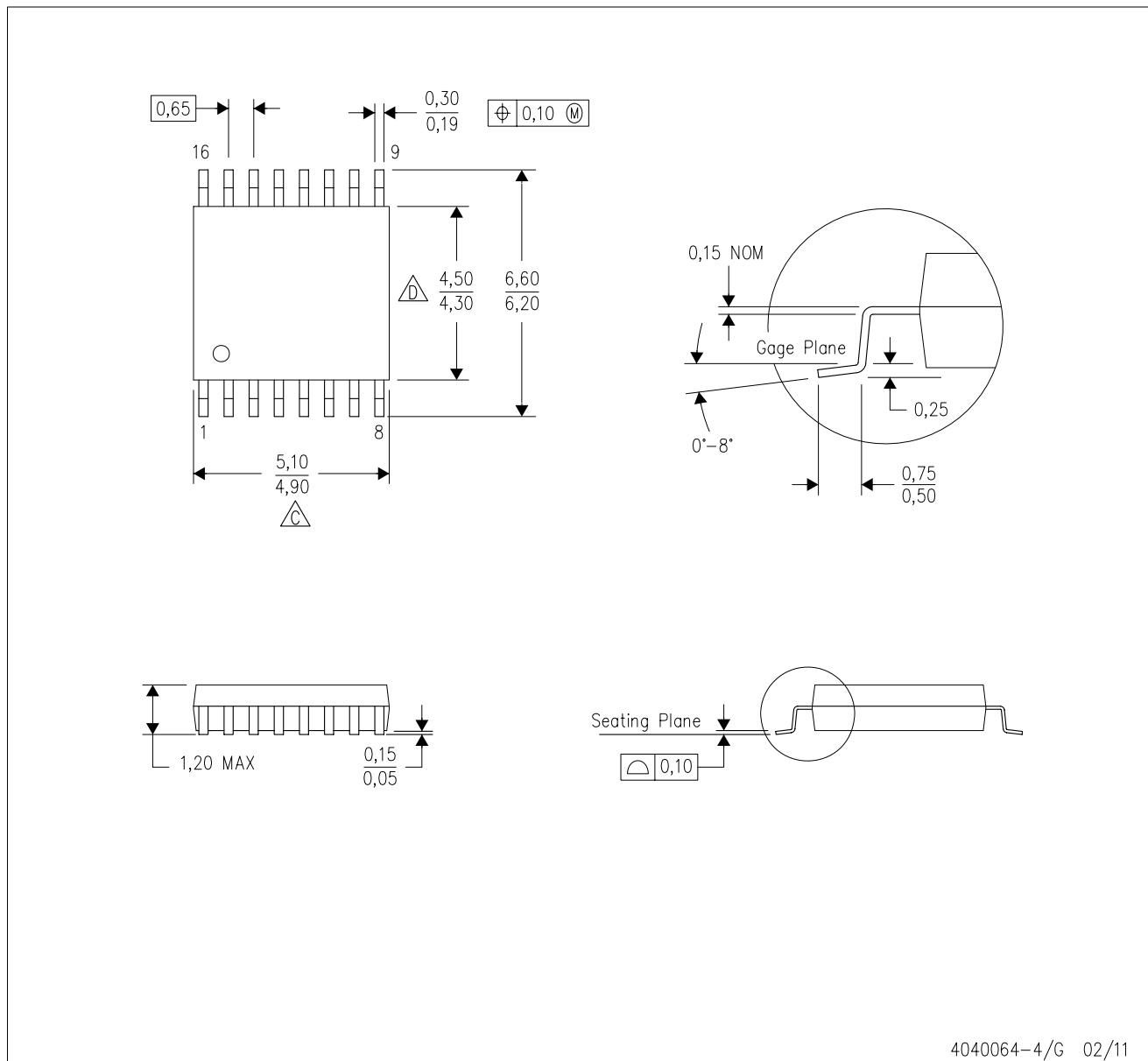0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         △C   Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
         △D   The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ 0,10 Ⓜ

16   9

4,50
4,30

6,60
6,20

1   8

5,10
4,90

Ⓒ

0,15 NOM

Gage Plane

0°−8°

0,25

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

⌂ 0,10

4040064−4/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B. This drawing is subject to change without notice.
         Ⓒ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
             not exceed 0,15 each side.
         Ⓓ Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
         E. Falls within JEDEC MO−153

PW (R−PDSO−G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

14x0,65

5,60

Stencil Openings
(Note D)

16x0,30

14x0,65

16x1,55

5,60

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,35

1,60

0,07
All Around

Example
Solder Mask Opening
(See Note E)

4211284−3/E 07/12

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Publication IPC−7351 is recommended for alternate designs.
          D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
             B.   This drawing is subject to change without notice.
             C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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