TOP252-262
TOPSwitch®-HX Family

Enhanced EcoSmart®, Integrated Off-Line Switcher with Advanced Feature Set and Extended Power Range

Product Highlights

Lower System Cost, Higher Design Flexibility

- Multi-mode operation maximizes efficiency at all loads
- New eSIP-7F and eSIP-7C packages
  - Low thermal impedance junction-to-case (2 °C per watt)
  - Low height is ideal for adapters where space is limited
  - Simple mounting using a clip to aid low cost manufacturing
  - Horizontal eSIP-7F package ideal for ultra low height adapter and monitor applications
  - Extended package creepage distance from DRAIN pin to adjacent pin and to heat sink
- No heatsink required up to 35 W using P, G and M packages with universal input voltage and up to 48 W at 230 VAC
- Output overvoltage protection (OVP) is user programmable for latching/non-latching shutdown with fast AC reset
  - Allows both primary and secondary sensing
- Line undervoltage (UV) detection prevents turn-off glitches
- Line overvoltage (OV) shutdown extends line surge limit
- Accurate programmable current limit
- Optimized line feed-forward for line ripple rejection
- 132 kHz frequency (254Y-258Y and all E/L packages) reduces transformer and power supply size
  - Half frequency option for video applications
- Frequency jittering reduces EMI filter cost

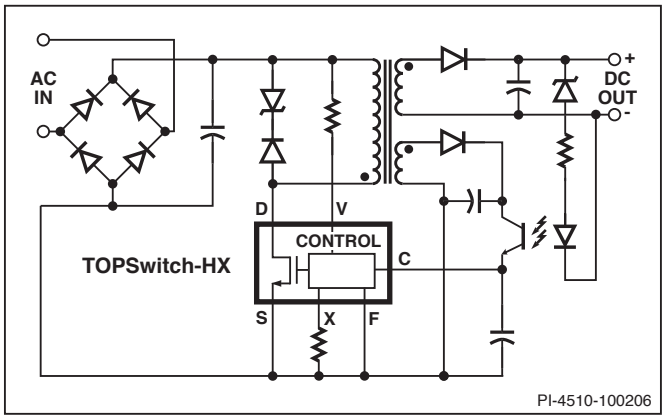


Figure 1. Typical Flyback Application.

- Heatsink is connected to SOURCE for low EMI
- Improved auto-restart delivers <3% of maximum power in short circuit and open loop fault conditions
- Accurate hysteretic thermal shutdown function automatically recovers without requiring a reset
- Fully integrated soft-start for minimum start-up stress
- Extended creepage between DRAIN and all other pins improves field reliability

Output Power Table

Product[5]	230 VAC ±15%[4]			85-265 VAC		
	Adapter[1]	Open Frame[2]	Peak[3]	Adapter[1]	Open Frame[2]	Peak[3]
TOP252PN/GN	9 W	15 W	21 W	6 W	10 W	13 W
TOP252MN			21 W			13 W
TOP253PN/GN	15 W	25 W	38 W	9 W	15 W	25 W
TOP253MN			43 W			29 W
TOP254PN/GN	16 W	28 W	47 W	11 W	20 W	30 W
TOP254MN			62 W			40 W
TOP255PN/GN	19 W	30 W	54 W	13 W	22 W	35 W
TOP255MN			81 W			52 W
TOP256PN/GN	21 W	34 W	63 W	15 W	26 W	40 W
TOP256MN			98 W			64 W
TOP257PN/GN	25 W	41 W	70 W	19 W	30 W	45 W
TOP257MN			119 W			78 W
TOP258PN/GN	29 W	48 W	77 W	22 W	35 W	50 W
TOP258MN			140 W			92 W

Product[5]	230 VAC ±15%		85-265 VAC	
	Adapter[1]	Open Frame[2]	Adapter[1]	Open Frame[2]
TOP252EN	10 W	21 W	6 W	13 W
TOP253EN	21 W	43 W	13 W	29 W
TOP254EN/YN	30 W	62 W	20 W	43 W
TOP255EN/YN	40 W	81 W	26 W	57 W
TOP255LN	40 W	81 W	26 W	57 W
TOP256EN/YN[7]	60 W	119 W	40 W	86 W
TOP256LN	60 W	88 W	40 W	64 W
TOP257EN/YN	85 W	157 W	55 W	119 W
TOP257LN	85 W	105 W	55 W	78 W
TOP258EN/YN	105 W	195 W	70 W	148 W
TOP258LN	105 W	122 W	70 W	92 W
TOP259EN/YN	128 W	238 W	80 W	171 W
TOP259LN	128 W	162 W	80 W	120 W
TOP260EN/YN	147 W	275 W	93 W	200 W
TOP260LN	147 W	190 W	93 W	140 W
TOP261EN/YN	177 W	333 W	118 W	254 W
TOP261LN	177 W	244 W	118 W	177 W
TOP262EN[6]	177 W	333 W	118 W	254 W
TOP262LN[6]	177 W	244 W	118 W	177 W

Table 1. Output Power Table. (for notes see page 2).

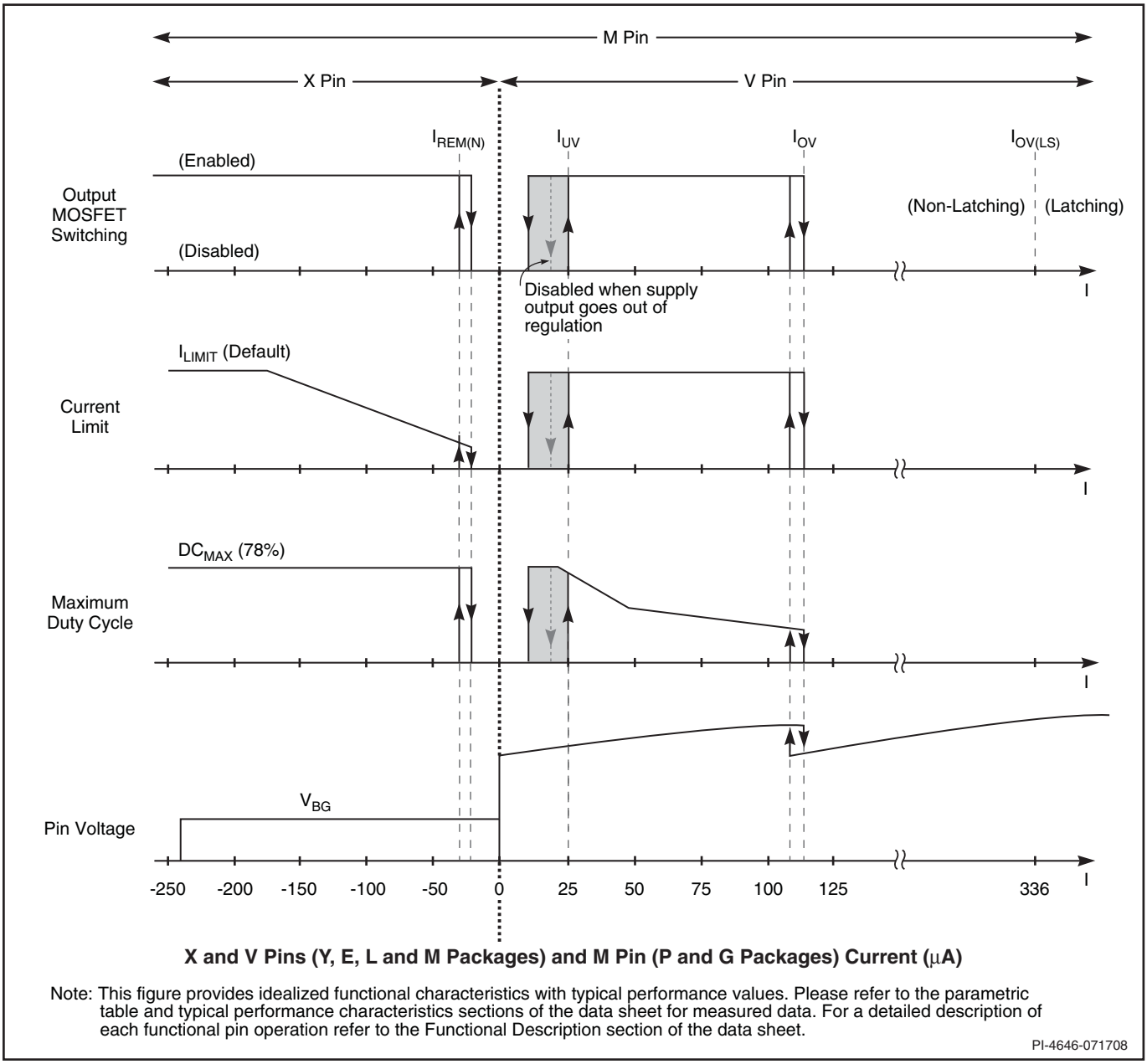


Figure 12. MULTI-FUNCTION (P and G package). VOLTAGE MONITOR and EXTERNAL CURRENT LIMIT (Y, E/L and M package) Pin Characteristics.

The circuit examples shown in Figures 41, 42 and 43 show a simple method for implementing the primary sensed over-voltage protection.

During a fault condition resulting from loss of feedback, output voltage will rapidly rise above the nominal voltage. The increase in output voltage will also result in an increase in the voltage at the output of the bias winding. A voltage at the output of the bias winding that exceeds of the sum of the voltage rating of the Zener diode connected from the bias winding output to the V-pin (or M-pin) and V-pin (or M-pin) voltage, will cause a current in excess of I_V or I_M to be injected into the V-pin (or M-pin), which will trigger the OVP feature.

The primary sensed OVP protection circuit shown in Figures 41, 42 and 43 is triggered by a significant rise in output voltage (and therefore bias winding voltage). If the power supply is operating under heavy load or low input line conditions when an open loop occurs, the output voltage may not rise significantly. Under these conditions, a latching shutdown will not occur until load or line conditions change. Nevertheless, the operation provides the desired protection by preventing significant rise in the output voltage when the line or load conditions do change. Primary side OVP protection with the TOPSwitch-HX in a typical application will prevent a nominal 12 V output from rising above approximately 20 V under open loop conditions. If greater accuracy is required, a secondary sensed OVP circuit is recommended.

Typical Uses of FREQUENCY (F) Pin

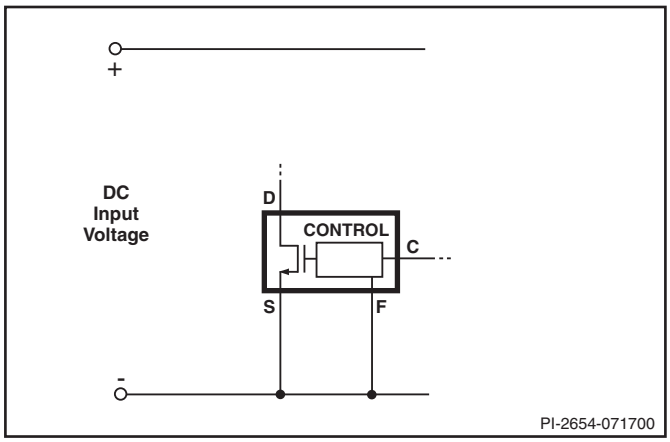


Figure 14. Full Frequency Operation (132 kHz).

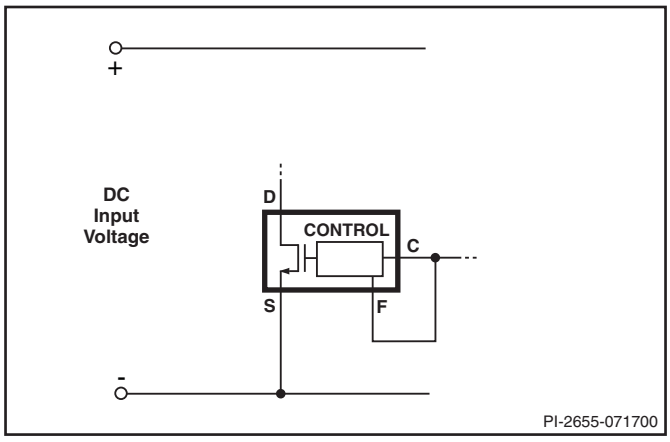


Figure 15. Half Frequency Operation (66 kHz).

Application Examples

A High Efficiency, 35 W, Dual Output - Universal Input Power Supply

The circuit in Figure 41 takes advantage of several of the TOPSwitch-HX features to reduce system cost and power supply size and to improve efficiency. This design delivers 35 W total continuous output power from a 90 VAC to 265 VAC input at an ambient of 50 ºC in an open frame configuration. A nominal efficiency of 84% at full load is achieved using TOP258P. With a DIP-8 package, this design provides 35 W continuous output power using only the copper area on the circuit board underneath the part as a heat sink. The different operating modes of the TOPSwitch-HX provide significant improvement in the no-load, standby, and light load performance of the power supply as compared to the previous generations of the TOPSwitch.

Resistors R3 and R4 provide line sensing, setting line UV at 100 VDC and line OV at 450 VDC.

Diode D5, together with resistors R6, R7, capacitor C6 and TVS VR1, forms a clamp network that limits the drain voltage of the TOPSwitch after the integrated MOSFET turns off. TVS VR1 provides a defined maximum clamp voltage and typically only conducts during fault conditions such as overload. This allows the RCD clamp (R6, R7, C6 and D5) to be sized for normal operation, thereby maximizing efficiency at light load. Should the feedback circuit fail, the output of the power supply may exceed regulation limits. This increased voltage at output will also result in an increased voltage at the output of the bias winding. Zener VR2 will break down and current will flow into the “M” pin of the TOPSwitch initiating a hysteretic overvoltage protection with automatic restart attempts. Resistor R5 will limit the current into the M pin to < 336 μA, thus setting hysteretic OVP. If latching OVP is desired, the value of R5 can be reduced to 20 Ω.

The output voltage is controlled using the amplifier TL431. Diode D9, capacitor C20 and resistor R16 form the soft finish circuit. At startup, capacitor C20 is discharged. As the output voltage starts rising, current flows through the optocoupler diode inside U2A, resistor R13 and diode D9 to charge capacitor C20. This provides feedback to the circuit on the primary side. The current in the optocoupler diode U2A gradually decreases as the capacitor C20 becomes charged and the control amplifier IC U3 becomes operational. This ensures that the output voltage increases gradually and settles to the final value without any overshoot. Resistor R16 ensures that the capacitor C20 is maintained charged at all times after startup, which effectively isolates C20 from the feedback circuit after startup. Capacitor C20 discharges through R16 when the supply shuts down.

Resistors R20, R21 and R18 form a voltage divider network. The output of this divider network is primarily dependent on the divider circuit formed using R20 and R21 and will vary to some extent for changes in voltage at the 15 V output due to the connection of resistor R18 to the output of the divider network. Resistor R19 and Zener VR3 improve cross regulation in case only the 5 V output is loaded, which results in the 15 V output operating at the higher end of the specification.

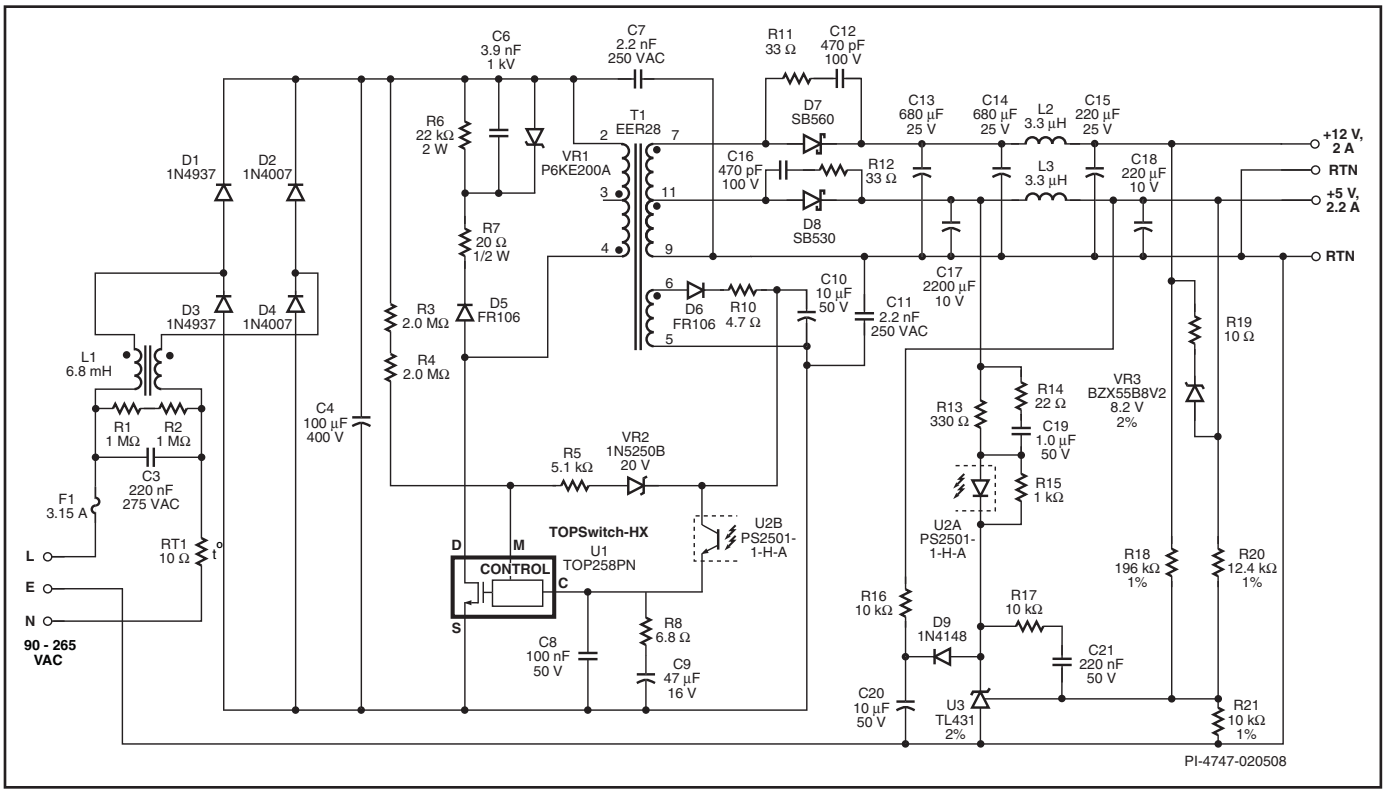


Figure 41. 35 W Dual Output Power Supply using TOP258PN.

A High Efficiency, 150 W, 250 – 380 VDC Input Power Supply

The circuit shown in Figure 42 delivers 150 W (19 V @ 7.7 A) at 84% efficiency using a TOP258Y from a 250 VDC to 380 VDC input. A DC input is shown, as typically at this power level a power factor correction stage would precede this supply, providing the DC input. Capacitor C1 provides local decoupling, necessary when the supply is remote from the main PFC output capacitor.

The flyback topology is still usable at this power level due to the high output voltage, keeping the secondary peak currents low enough so that the output diode and capacitors are reasonably sized. In this example, the TOP258YN is at the upper limit of its power capability.

Resistors R3, R6 and R7 provide output power limiting, maintaining relatively constant overload power with input voltage. Line sensing is implemented by connecting a 4 MΩ resistor from the V pin to the DC rail. Resistors R4 and R5 together form the 4 MΩ line sense resistor. If the DC input rail rises above 450 VDC, then TOPSwitch-HX will stop switching until the voltage returns to normal, preventing device damage.

Due to the high primary current, a low leakage inductance transformer is essential. Therefore, a sandwich winding with a copper foil secondary was used. Even with this technique, the leakage inductance energy is beyond the power capability of a simple Zener clamp. Therefore, R1, R2 and C3 are added in parallel to VR1 and VR3, two series TVS diodes being used to reduce dissipation. During normal operation, very little power is dissipated by VR1 and VR3, the leakage energy instead being dissipated by R1 and R2. However, VR1 and VR3 are essential to limit the peak drain voltage during start-up and/or overload conditions to below the 700 V rating of the TOPSwitch-HX MOSFET. The schematic shows an additional turn-off snubber circuit consisting of R20, R21, R22, D5 and C18. This reduces turn-off losses in the TOPSwitch-HX.

The secondary is rectified and smoothed by D2, D3 and C5, C6, C7 and C8. Two windings are used and rectified with separate diodes D2 and D3 to limit diode dissipation. Four capacitors are used to ensure their maximum ripple current specification is not exceeded. Inductor L1 and capacitors C15 and C16 provide switching noise filtering.

Output voltage is controlled using a TL431 reference IC and R15, R16 and R17 to form a potential divider to sense the output voltage. Resistor R12 and R24 together limit the optocoupler LED current and set overall control loop DC gain. Control loop compensation is achieved using components C12, C13, C20 and R13. Diode D6, resistor R23 and capacitor C19 form a soft finish network. This feeds current into the control pin prior to output regulation, preventing output voltage overshoot and ensuring startup under low line, full load conditions.

Sufficient heat sinking is required to keep the TOPSwitch-HX device below 110 °C when operating under full load, low line and maximum ambient temperature. Airflow may also be required if a large heat sink area is not acceptable.

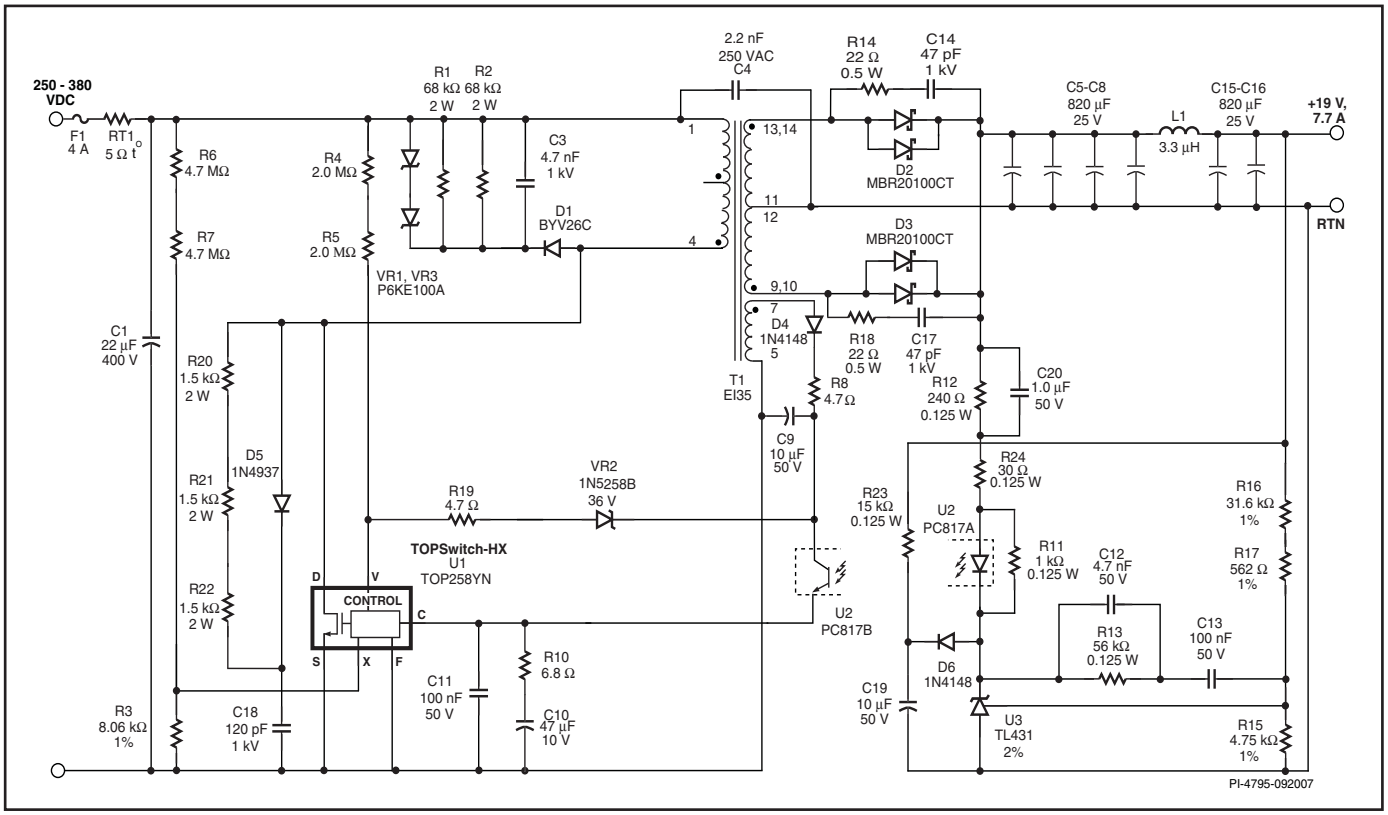


Figure 42. 150 W, 19 V Power Supply using TOP258YN.

A High Efficiency, 20 W continuous – 80 W Peak, Universal Input Power Supply

The circuit shown in Figure 43 takes advantage of several of TOPSwitch-HX features to reduce system cost and power supply size and to improve power supply efficiency while delivering significant peak power for a short duration. This design delivers continuous 20 W and peak 80 W at 32 V from an 90 VAC to 264 VAC input. A nominal efficiency of 82% at full load is achieved using TOP258MN. The M-package part has an optimized current limit to enable design of power supplies capable of delivering high power for a short duration.

Resistor R12 sets the current limit of the part. Resistors R11 and R14 provide line feed forward information that reduces the current limit with increasing DC bus voltage, thereby maintaining a constant overload power level with increasing line voltage. Resistors R1 and R2 implement the line undervoltage and over-voltage function and also provide feed forward compensation for reducing line frequency ripple at the output. The overvoltage feature inhibits TOPSwitch-HX switching during a line surge extending the high voltage withstand to 700 V without device damage.

The snubber circuit comprising of VR7, R17, R25, C5 and D2 limits the maximum drain voltage and dissipates energy stored in the leakage inductance of transformer T1. This clamp configuration maximizes energy efficiency by preventing C5 from discharging below the value of VR7 during the lower frequency operating modes of TOPSwitch-HX. Resistor R25 damps high frequency ringing for reduced EMI.

A combined output overvoltage and over power protection circuit is provided via the latching shutdown feature of TOPSwitch-HX and R20, C9, R22 and VR5. Should the bias winding output voltage across C13 rise due to output overload or an open loop fault (opto coupler failure), then VR5 conducts triggering the latching shutdown. To prevent false triggering due to short duration overload, a delay is provided by R20, R22 and C9.

To reset the supply following a latching shutdown, the V pin must fall below the reset threshold. To prevent the long reset delay associated with the input capacitor discharging, a fast AC reset circuit is used. The AC input is rectified and filtered by D13 and C30. While the AC supply is present, Q3 is on and Q1 is off, allowing normal device operation. However when AC is removed, Q1 pulls down the V pin and resets the latch. The supply will then return to normal operation when AC is again applied.

Transistor Q2 provides an additional lower UV threshold to the level programmed via R1, R2 and the V pin. At low input AC voltage, Q2 turns off, allowing the X pin to float and thereby disabling switching.

A simple feedback circuit automatically regulates the output voltage. Zener VR3 sets the output voltage together with the voltage drop across series resistor R8, which sets the DC gain of the circuit. Resistors R10 and C28 provide a phase boost to improve loop bandwidth.

Diodes D6 and D7 are low-loss Schottky rectifiers, and capacitor C20 is the output filter capacitor. Inductor L3 is a common mode choke to limit radiated EMI when long output cables are used and the output return is connected to safety earth ground. Example applications where this occurs include PC peripherals, such as inkjet printers.

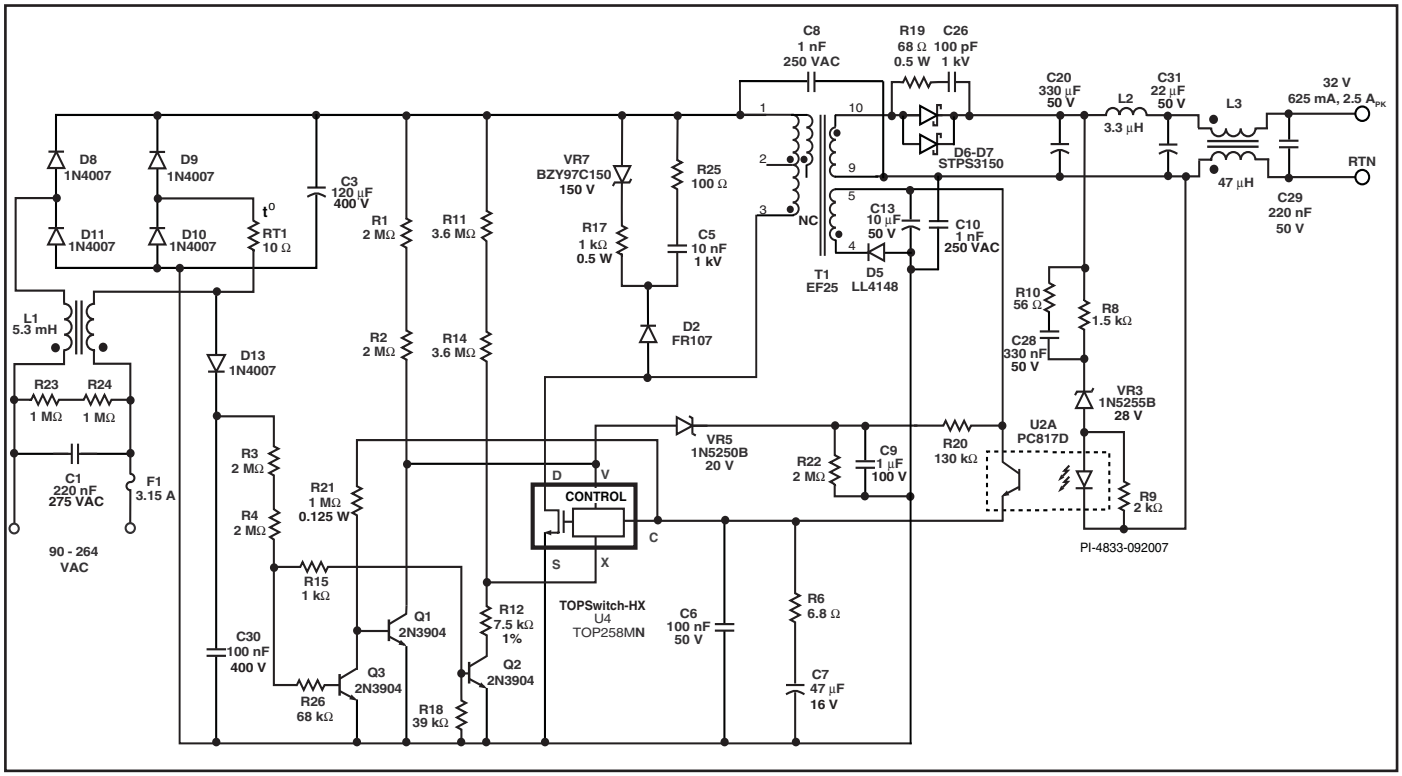


Figure 43. 20 W Continuous, 80 W Peak, Universal Input Power Supply using TOP258MN.

A High Efficiency, 65 W, Universal Input Power Supply
The circuit shown in Figure 44 delivers 65 W (19 V @ 3.42 A) at 88% efficiency using a TOP260EN operating over an input voltage range of 90 VAC to 265 VAC.

Capacitors C1 and C6 and inductors L1 and L2 provide common mode and differential mode EMI filtering. Capacitor C2 is the bulk filter capacitor that ensures low ripple DC input to the flyback converter stage. Capacitor C4 provides decoupling for switching currents reducing differential mode EMI.

In this example, the TOP260EN is used at reduced current limit to improve efficiency.

Resistors R5, R6 and R7 provide power limiting, maintaining relatively constant overload power with input voltage. Line sensing is implemented by connecting a 4 MΩ impedance from the V pin to the DC rail. Resistors R3 and R4 together form the 4 MΩ line sense resistor. If the DC input rail rises above 450 VDC, then TOPSwitch-HX will stop switching until the voltage returns to normal, preventing device damage.

This circuit features a high efficiency clamp network consisting of diode D1, zener VR1, capacitor C5 together with resistors R8 and R9. The snubber clamp is used to dissipate the energy of the leakage reactance of the transformer. At light load levels, very little power is dissipated by VR1 improving efficiency as compared to a conventional RCD clamp network.

The secondary output from the transformer is rectified by diode D2 and filtered by capacitors C13 and C14. Ferrite Bead L3 and capacitors C15 form a second stage filter and effectively reduce the switching noise to the output.

Output voltage is controlled using a LM431 reference IC. Resistor R19 and R20 form a potential divider to sense the output voltage. Resistor R16 limits the optocoupler LED current and sets the overall control loop DC gain. Control loop compensation is achieved using C18 and R21. The components connected to the control pin on the primary side C8, C9 and R15 set the low frequency pole and zero to further shape the control loop response. Capacitor C17 provides a soft finish during startup. Optocoupler U2 is used for isolation of the feedback signal.

Diode D4 and capacitor C10 form the bias winding rectifier and filter. Should the feedback loop break due to a defective component, a rising bias winding voltage will cause the zener VR2 to break down and trigger the over voltage protection which will inhibit switching.

An optional secondary side over voltage protection feature which offers higher precision (as compared to sensing via the bias winding) is implemented using VR3, R18 and U3. Excess voltage at the output will cause current to flow through the optocoupler U3 LED which in turn will inject current in the V-pin through resistor R13, thereby triggering the over voltage protection feature.

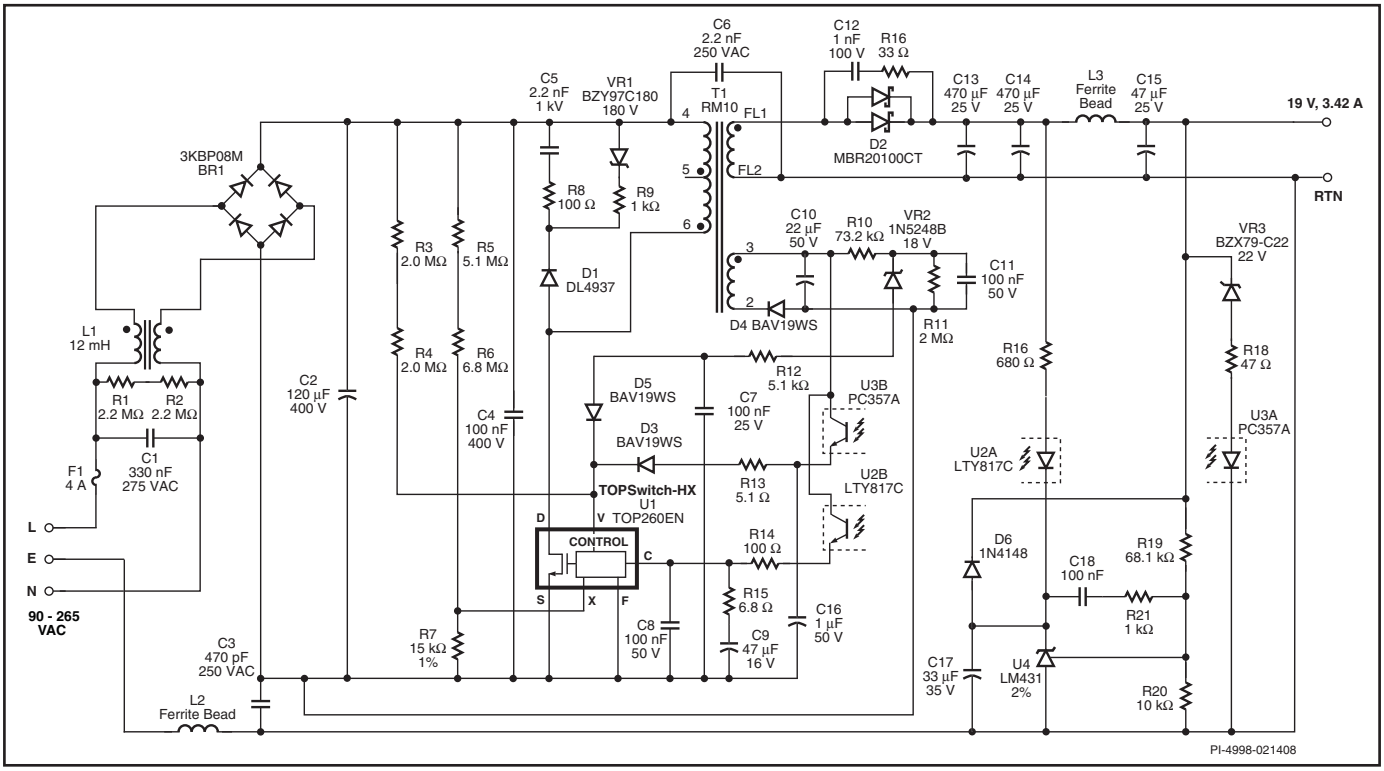


Figure 44. 65 W, 19 V Power Supply Using TOP260EN.

Key Application Considerations

TOPSwitch-HX vs. TOPSwitch-GX

Table 4 compares the features and performance differences between TOPSwitch-HX and TOPSwitch-GX. Many of the new features eliminate the need for additional discrete components. Other features increase the robustness of design, allowing cost savings in the transformer and other power components.

TOPSwitch-HX vs. TOPSwitch-GX

Function	TOPSwitch-GX	TOPSwitch-HX	TOPSwitch-HX Advantages
EcoSmart	Linear frequency reduction to 30 kHz (@ 132 kHz) for duty cycles < 10%	Multi-mode operation with linear frequency reduction to 30 kHz (@ 132 kHz) and multi-cycle modulation (virtually no audible noise)	• Improved efficiency over load (e.g. at 25% load point) • Improved standby efficiency • Improved no-load consumption
Output Overvoltage Protection (OVP)	Not available	User programmable primary or secondary hysteretic or latching OVP	• Protects power supply output during open loop fault • Maximum design flexibility
Line Feed-Forward with Duty Cycle Reduction	Linear reduction	Dual slope reduction with lower, more accurate onset point	• Improved line ripple rejection • Smaller DC bus capacitor
Switching Frequency DIP-8 Package	132 kHz	66 kHz	• Increased output power for given MOSFET size due to higher efficiency
Lowest MOSFET On Resistance in DIP-8 Package	3.0 Ω (TOP246P)	1.8 Ω (TOP258P)	• Increased output power in designs without external heatsink
I^2f Trimming	Not available	-10% / +20%	• Increased output power for given core size • Reduced over-load power
Auto-restart Duty Cycle	5.6%	2%	• Reduced delivered average output power during open loop faults
Frequency Jitter	±4 kHz @ 132 kHz ±2 kHz @ 66 kHz	±5 kHz @ 132 kHz ±2.5 kHz @ 66 kHz	• Reduced EMI filter cost
Thermal Shutdown	130 °C to 150 °C	135 °C to 150 °C	• Increased design margin
External Current Limit	30%-100% of I_{LIMIT}	30%-100% of I_{LIMIT}, additional trim at 0.7 × I_{LIMIT}	• Reduced tolerances when current limit is set externally
Line UV Detection Threshold	50 µA (2 MΩ sense impedance)	25 µA (4 MΩ sense impedance)	• Reduced dissipation for lower no-load consumption
Soft-Start	10 ms duty cycle and current limit ramp	17 ms sweep through multi-mode characteristic	• Reduced peak current and voltage component stress at startup • Smooth output voltage rise

Table 4. Comparison Between TOPSwitch-GX and TOPSwitch-HX.

TOPSwitch-HX Design Considerations

Power Table

The data sheet power table (Table 1) represents the maximum practical continuous output power based on the following conditions:

1. 12 V output.
2. Schottky or high efficiency output diode.
3. 135 V reflected voltage (V_{OR}) and efficiency estimates.
4. A 100 VDC minimum for 85-265 VAC and 250 VDC minimum for 230 VAC.
5. Sufficient heat sinking to keep device temperature ≤100 °C.
6. Power levels shown in the power table for the M/P package device assume 6.45 cm^2 of 610 g/m^2 copper heat sink area in an enclosed adapter, or 19.4 cm^2 in an open frame.

The provided peak power depends on the current limit for the respective device.

TOPSwitch-HX Selection

Selecting the optimum TOPSwitch-HX depends upon required maximum output power, efficiency, heat sinking constraints, system requirements and cost goals. With the option to externally reduce current limit, an Y, E/L or M package TOPSwitch-HX may be used for lower power applications where higher efficiency is needed or minimal heat sinking is available.

Input Capacitor

The input capacitor must be chosen to provide the minimum DC voltage required for the TOPSwitch-HX converter to maintain regulation at the lowest specified input voltage and maximum output power. Since TOPSwitch-HX has a high DC_{MAX} limit and an optimized dual slope line feed forward for ripple rejection, it is possible to use a smaller input capacitor. For TOPSwitch-HX, a capacitance of 2 µF per watt is possible for universal input with an appropriately designed transformer.

Primary Clamp and Output Reflected Voltage V_{OR}

A primary clamp is necessary to limit the peak TOPSwitch-HX drain to source voltage. A Zener clamp requires few parts and takes up little board space. For good efficiency, the clamp Zener should be selected to be at least 1.5 times the output reflected voltage V_{OR}, as this keeps the leakage spike conduction time short. When using a Zener clamp in a universal input application, a V_{OR} of less than 135 V is recommended to allow for the absolute tolerances and temperature variations of the Zener. This will ensure efficient operation of the clamp circuit and will also keep the maximum drain voltage below the rated breakdown voltage of the TOPSwitch-HX MOSFET. A high V_{OR} is required to take full advantage of the wider DC_{MAX} of TOPSwitch-HX. An RCD clamp provides tighter clamp voltage tolerance than a Zener clamp and allows a VOR as high as 150 V. RCD clamp dissipation can be minimized by reducing the external current limit as a function of input line voltage (see Figures 23 and 36). The RCD clamp is more cost effective than the Zener clamp but requires more careful design (see Quick Design Checklist).

Output Diode

The output diode is selected for peak inverse voltage, output current, and thermal conditions in the application (including heat sinking, air circulation, etc.). The higher DC_{MAX} of TOPSwitch-HX, along with an appropriate transformer turns ratio, can allow the use of a 80 V Schottky diode for higher efficiency on output voltages as high as 15 V (see Figure 41).

Bias Winding Capacitor

Due to the low frequency operation at no-load, a 10 µF bias winding capacitor is recommended.

Soft-Start

Generally, a power supply experiences maximum stress at start-up before the feedback loop achieves regulation. For a period of 17 ms, the on-chip soft-start linearly increases the drain peak current and switching frequency from their low starting values to their respective maximum values. This causes the output voltage to rise in an orderly manner, allowing time for the feedback loop to take control of the duty cycle. This reduces the stress on the TOPSwitch-HX MOSFET, clamp circuit and output diode(s), and helps prevent transformer saturation during start-up. Also, soft-start limits the amount of output voltage overshoot and, in many applications, eliminates the need for a soft-finish capacitor.

EMI

The frequency jitter feature modulates the switching frequency over a narrow band as a means to reduce conducted EMI peaks associated with the harmonics of the fundamental switching frequency. This is particularly beneficial for average detection mode. As can be seen in Figure 45, the benefits of jitter increase with the order of the switching harmonic due to an increase in frequency deviation. Devices in the P, G or M package and TOP259-261YN operate at a nominal switching frequency of 66 kHz. The FREQUENCY pin of devices in the TOP254-258 Y and E packages offer a switching frequency option of 132 kHz or 66 kHz. In applications that require heavy snubber on the drain node for reducing high frequency radiated noise (for example, video noise sensitive applications such as VCRs, DVDs, monitors, TVs, etc.), operating at 66 kHz will reduce snubber loss, resulting in better efficiency. Also, in applications where transformer size is not a concern, use of the 66 kHz option will provide lower EMI and higher efficiency. Note that the second harmonic of 66 kHz is still below 150 kHz, above which the conducted EMI specifications get much tighter. For 10 W or below, it is possible to use a simple inductor in place of a more costly AC input common mode choke to meet worldwide conducted EMI limits.

Transformer Design

It is recommended that the transformer be designed for maximum operating flux density of 3000 Gauss and a peak flux density of 4200 Gauss at maximum current limit. The turns ratio should be chosen for a reflected voltage (V_{OR}) no greater than 135 V when using a Zener clamp or 150 V (max) when using an RCD clamp with current limit reduction with line voltage (overload protection). For designs where operating current is significantly lower than the default current limit, it is recommended to use an externally set current limit close to the operating peak current to reduce peak flux density and peak power (see Figures 22 and 35). In most applications, the tighter current limit tolerance, higher switching frequency and soft-start features of TOPSwitch-HX contribute to a smaller transformer when compared to TOPSwitch-GX.

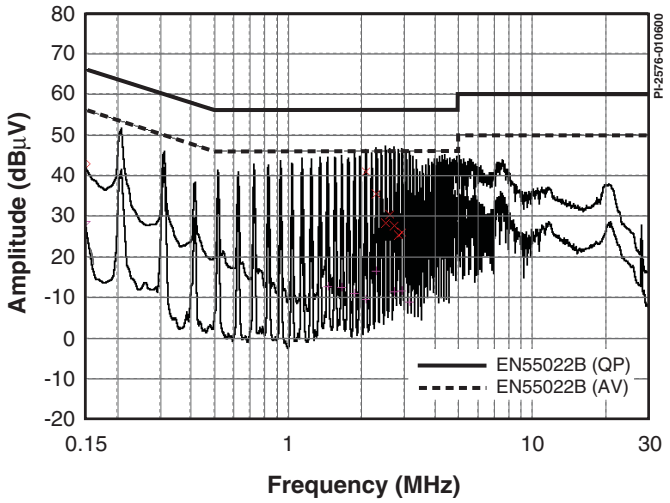


Figure 45a. Fixed Frequency Operation Without Jitter.

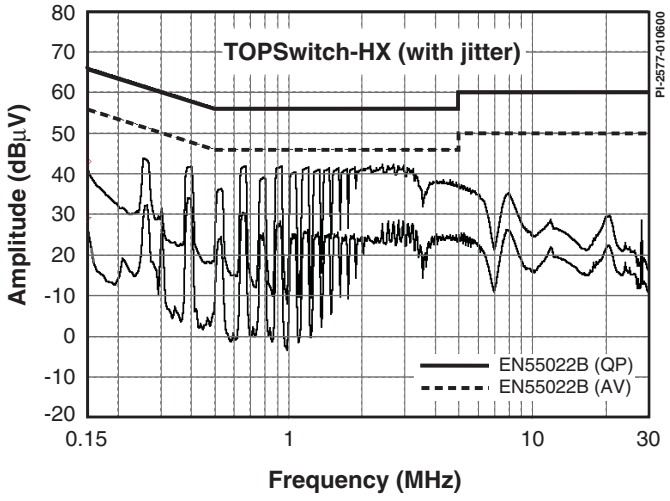


Figure 45b. TOPSwitch-HX Full Range EMI Scan (132 kHz With Jitter) With Identical Circuitry and Conditions.

Standby Consumption

Frequency reduction can significantly reduce power loss at light or no load, especially when a Zener clamp is used. For very low secondary power consumption, use a TL431 regulator for feedback control. A typical TOPSwitch-HX circuit automatically enters MCM mode at no load and the low frequency mode at light load, which results in extremely low losses under no-load or standby conditions.

High Power Designs

The TOPSwitch-HX family contains parts that can deliver up to 333 W. High power designs need special considerations. Guidance for high power designs can be found in the Design Guide for TOPSwitch-HX (AN-43).

TOPSwitch-HX Layout Considerations

The TOPSwitch-HX has multiple pins and may operate at high power levels. The following guidelines should be carefully followed.

Primary Side Connections

Use a single point (Kelvin) connection at the negative terminal of the input filter capacitor for the TOPSwitch-HX SOURCE pin and bias winding return. This improves surge capabilities by returning surge currents from the bias winding directly to the input filter capacitor. The CONTROL pin bypass capacitor should be located as close as possible to the SOURCE and CONTROL pins, and its SOURCE connection trace should not be shared by the main MOSFET switching currents. All SOURCE pin referenced components connected to the MULTI-FUNCTION (M-pin), VOLTAGE MONITOR (V-pin) or EXTERNAL CURRENT LIMIT (X-pin) pins should also be located closely between their respective pin and SOURCE. Once again, the SOURCE connection trace of these components should not be shared by the main MOSFET switching currents. It is very critical that SOURCE pin switching currents are returned to the input capacitor negative terminal through a separate trace that is not shared by the components connected to CONTROL, MULTI-FUNCTION, VOLTAGE MONITOR or EXTERNAL CURRENT LIMIT pins. This is because the SOURCE pin is also the controller ground reference pin. Any traces to the M, V or X pins should be kept as short as possible and away from the DRAIN trace to prevent noise coupling. VOLTAGE MONITOR resistors (R1 and R2 in Figures 46, 47, 48, R3 and R4 in Figure 49, and R14 in Figure 50) should be located close to the M or V pin to minimize the trace length on the M or V pin side. Resistors connected to the M, V or X pin should be connected as close to the bulk cap positive terminal as possible while routing these connections away from the power switching circuitry. In addition to the 47 µF CONTROL pin capacitor, a high frequency bypass capacitor in parallel may be used for better noise immunity. The feedback optocoupler output should also be located close to the CONTROL and SOURCE pins of TOPSwitch-HX.

Y-Capacitor

The Y-capacitor should be connected close to the secondary output return pin(s) and the positive primary DC input pin of the transformer.

Heat Sinking

The tab of the Y package (TO-220C) and E package (eSIP-7C) and L package (eSIP-7F) are internally electrically tied to the SOURCE pin. To avoid circulating currents, a heat sink attached to the tab should not be electrically tied to any primary ground/source nodes on the PC board. When using a P (DIP-8), G (SMD-8) or M (DIP-10) package, a copper area underneath the package connected to the SOURCE pins will act as an effective heat sink. On double sided boards, topside and bottom side areas connected with vias can be used to increase the effective heat sinking area. In addition, sufficient copper area should be provided at the anode and cathode leads of the output diode(s) for heat sinking. In Figures 46 to 50 a narrow trace is shown between the output rectifier and output filter capacitor. This trace acts as a thermal relief between the rectifier and filter capacitor to prevent excessive heating of the capacitor.

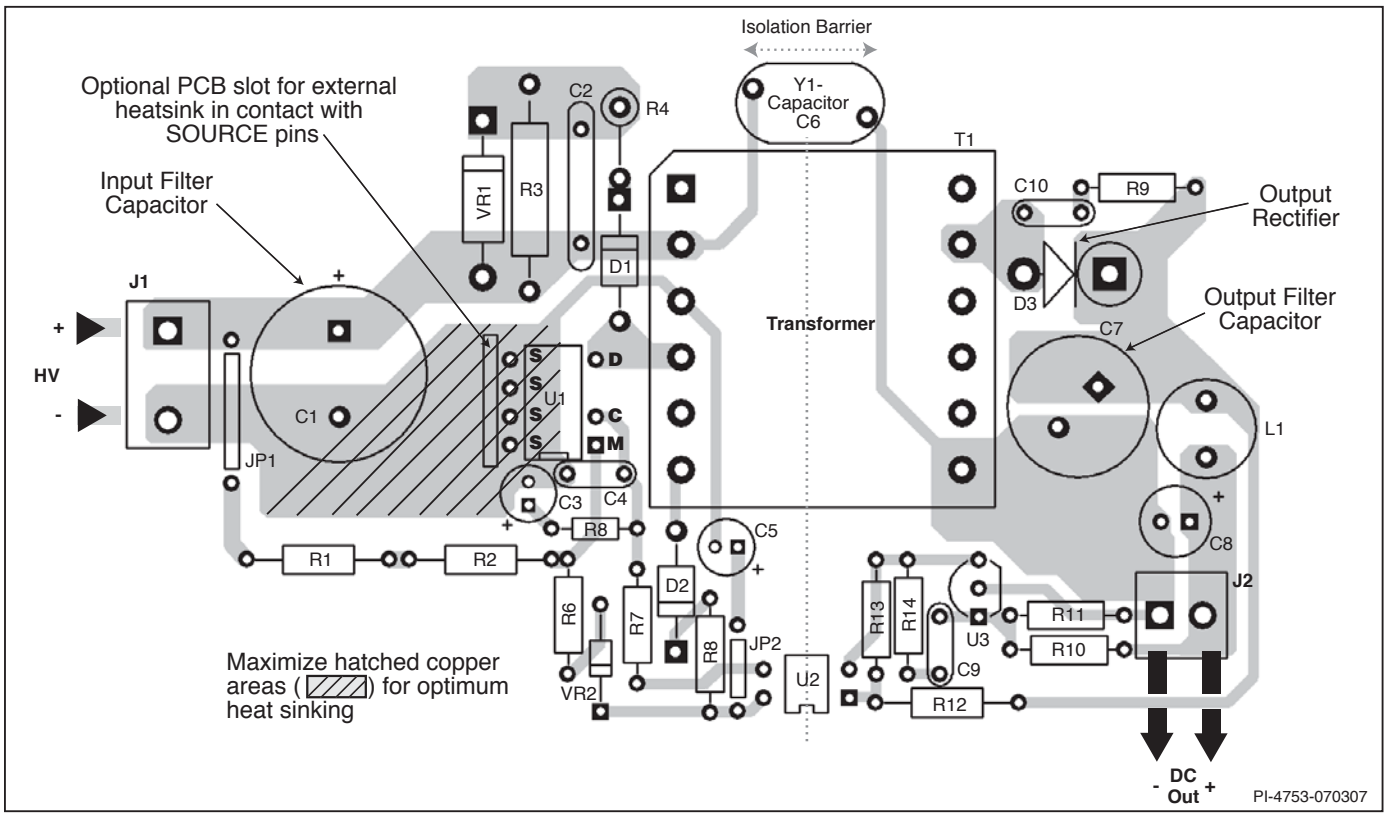


Figure 46. Layout Considerations for TOPSwitch-HX Using P-Package.

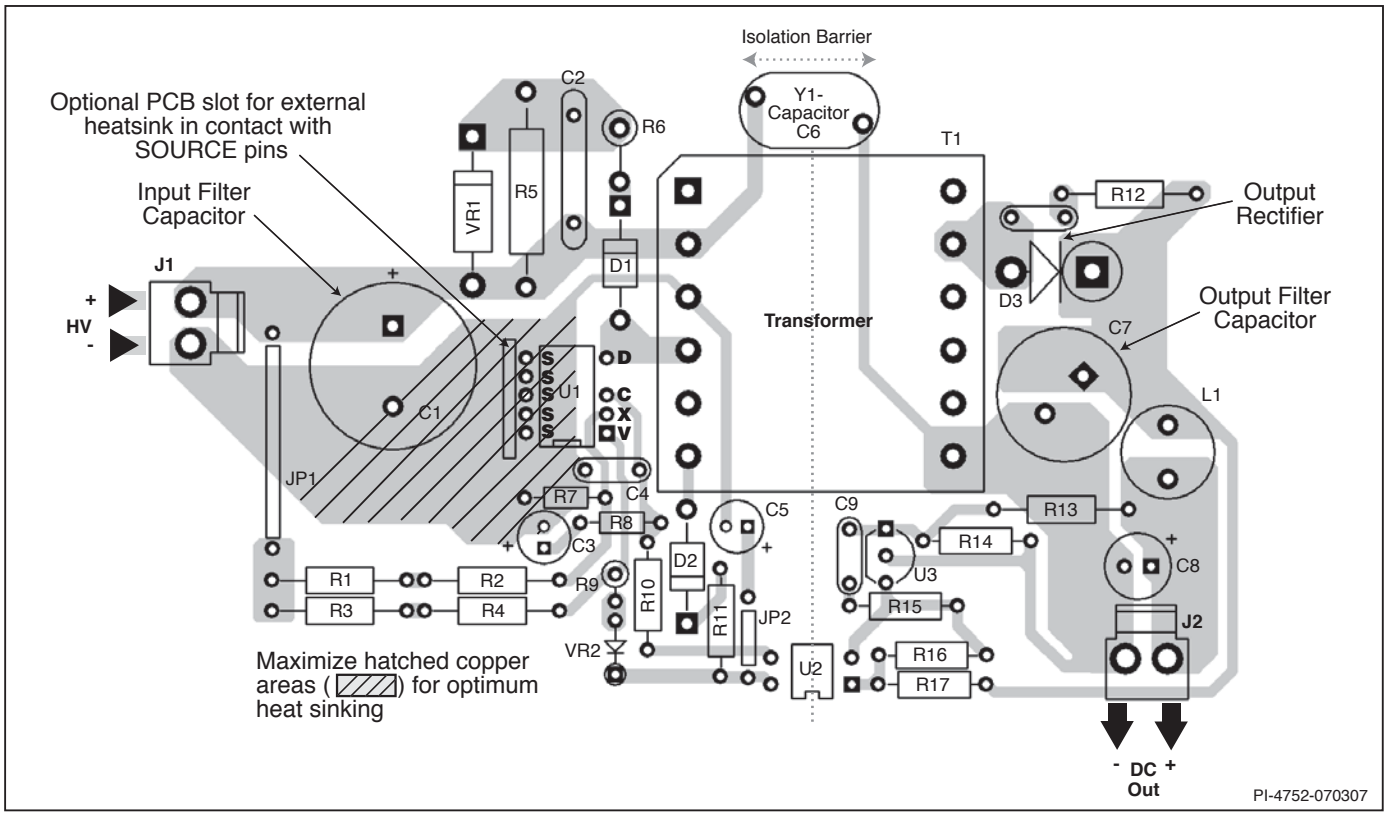


Figure 47. Layout Considerations for TOPSwitch-HX Using M-Package.

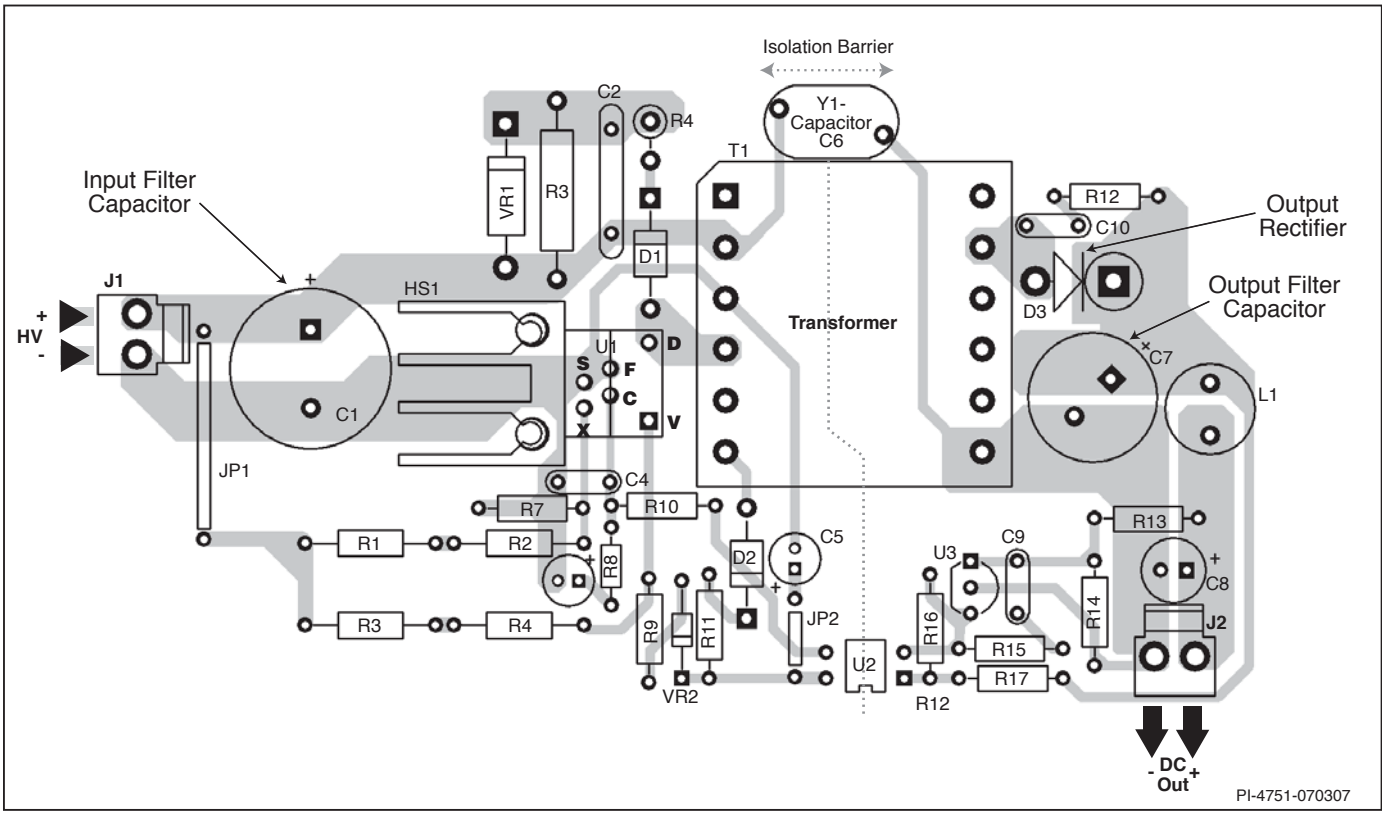


Figure 48. Layout Considerations for TOPSwitch-HX Using TOP254-258 Y-Package.

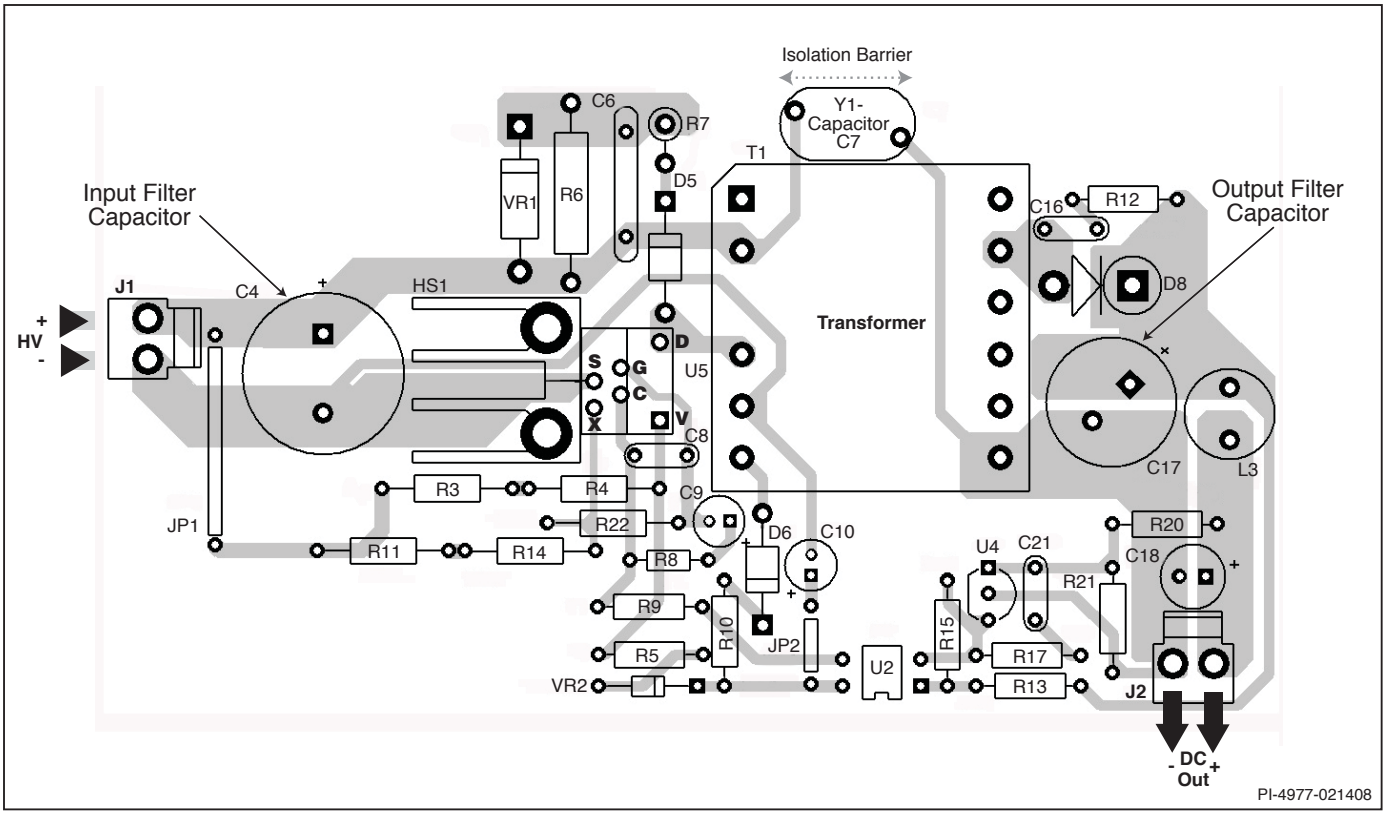


Figure 49. Layout Considerations for TOPSwitch-HX Using TOP259-261 Y-Package.

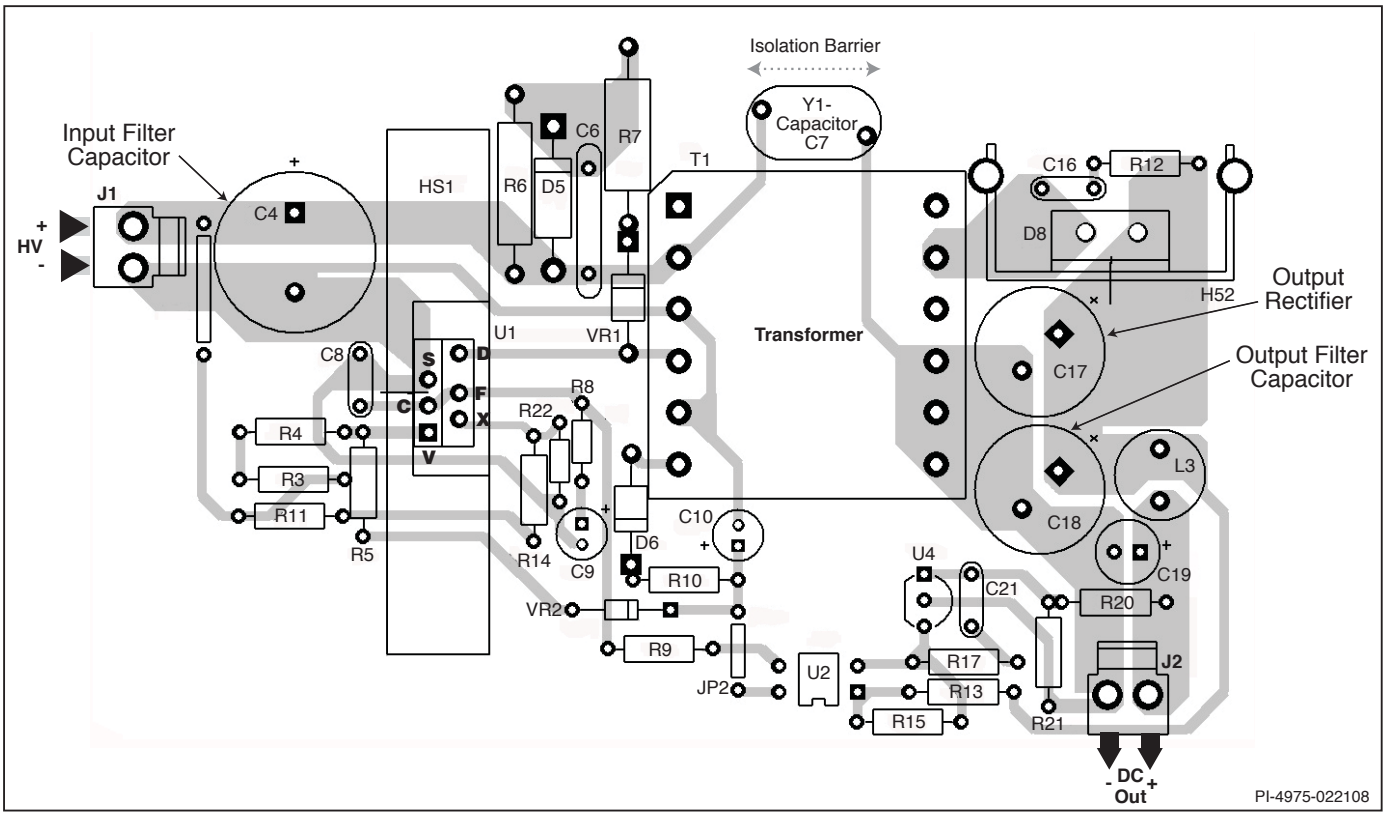


Figure 50a. Layout Considerations for TOPSwitch-HX Using E-Package and Operating at 66 kHz.

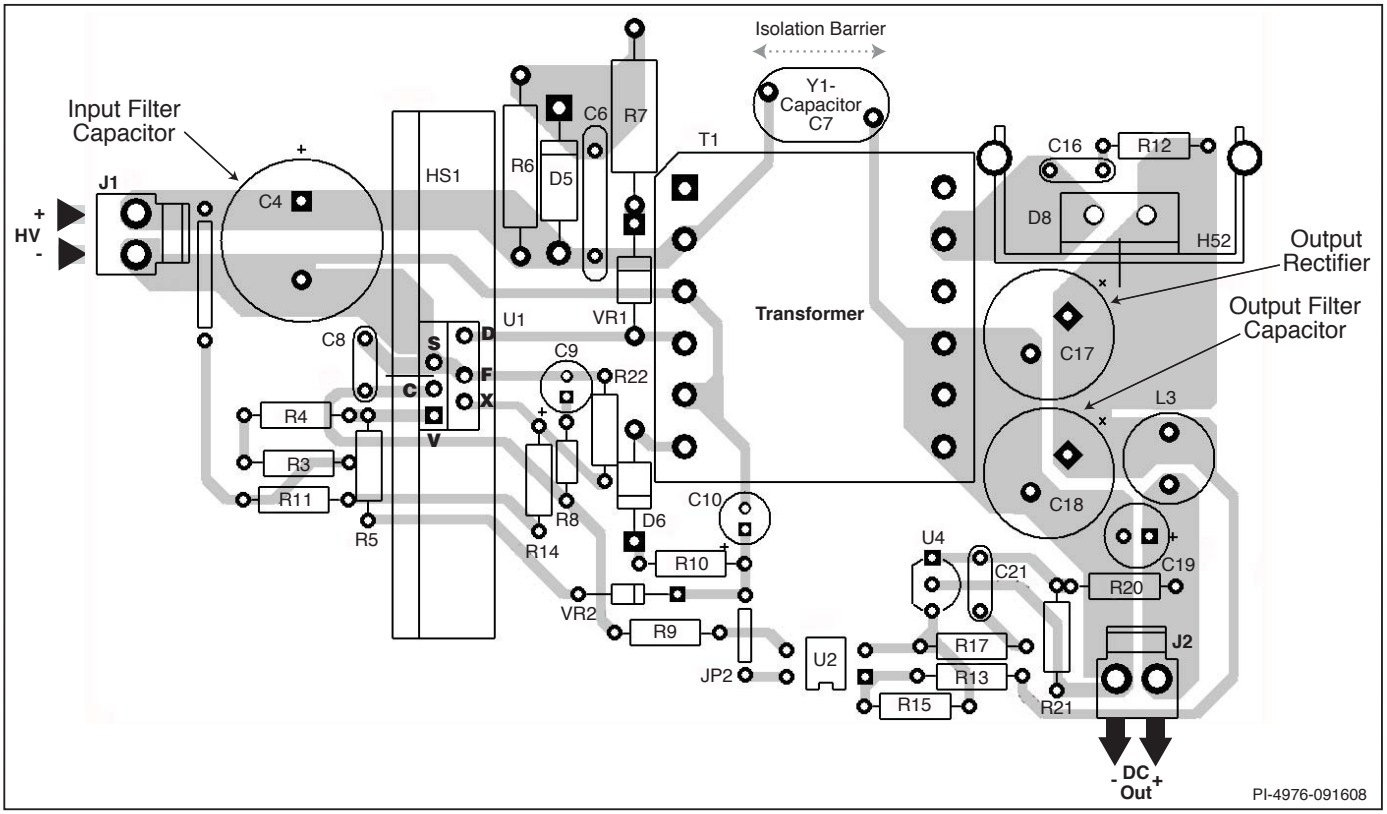
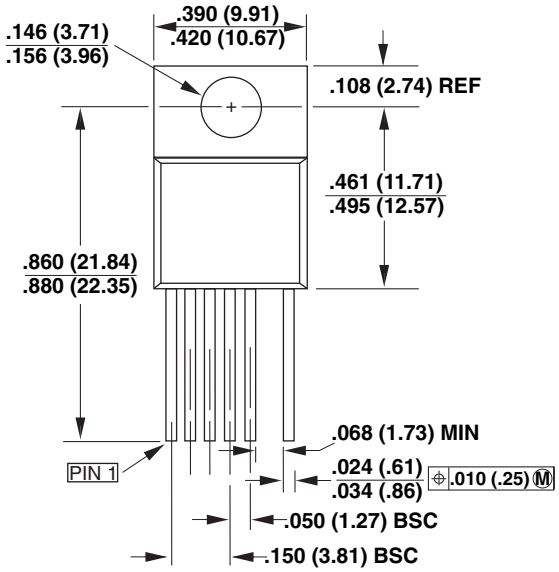
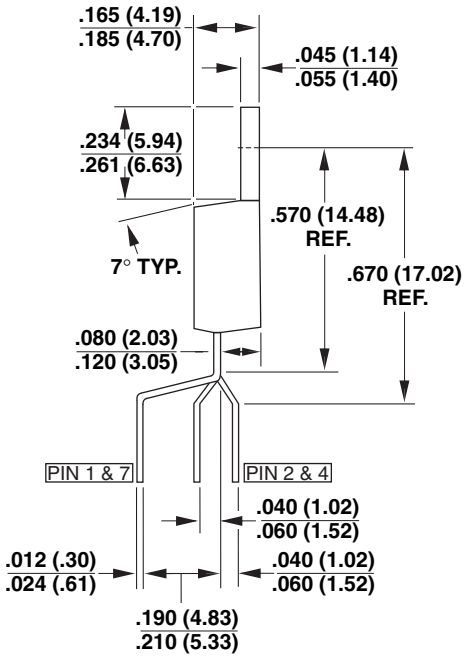


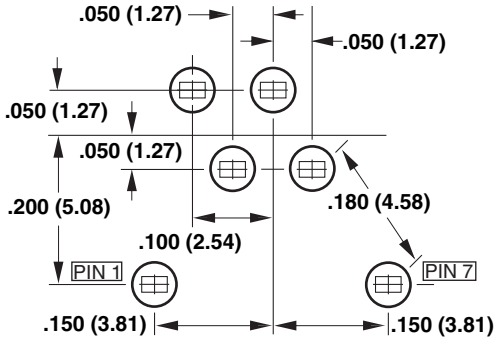
Figure 50b. Layout Considerations for TOPSwitch-HX Using E-Package and Operating at 132 kHz.

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions (cont.)							
External Bias Current	I_B	132 kHz Operation	TOP252-255	1.0	1.6	2.2	mA
			TOP256-258	1.3	1.9	2.5	
			TOP259-262	1.6	2.2	2.9	
CONTROL Current at 0% Duty Cycle	$I_{C(OFF)}$	66 kHz Operation	TOP252-255		4.4	5.8	mA
			TOP256-258		4.7	6.1	
			TOP259-262		5.1	6.5	
		132 kHz Operation	TOP252-255		4.6	6.0	
			TOP256-258		5.1	6.5	
			TOP259-262		6.0	7.4	
Dynamic Impedance	Z_C	I_C = 4 mA; T_J = 25 °C, See Figure 52		10	18	22	Ω
Dynamic Impedance Temperature Drift					0.18		%/°C
CONTROL Pin Internal Filter Pole					7		kHz
Upper Peak Current to Set Current Limit Ratio	$k_{PS(UPPER)}$	T_J = 25 °C See Note B		50	55	60	%
Lower Peak Current to Set Current Limit Ratio	$k_{PS(LOWER)}$	T_J = 25 °C See Note B			25		%
Multi-Cycle-Modulation Switching Frequency	$f_{MCM(MIN)}$	T_J = 25 °C			30		kHz
Minimum Multi-Cycle-Modulation On Period	$T_{MCM(MIN)}$	T_J = 25 °C			135		µs
Shutdown/Auto-Restart							
Control Pin Charging Current	$I_{C(CH)}$	T_J = 25 °C	V_C = 0 V	-5.0	-3.5	-1.0	mA
			V_C = 5 V	-3.0	-1.8	-0.6	
Charging Current Temperature Drift		See Note A			0.5		%/°C
Auto-Restart Upper Threshold Voltage	$V_{C(AR)U}$				5.8		V
Auto-Restart Lower Threshold Voltage	$V_{C(AR)L}$			4.5	4.8	5.1	V
Multi-Function (M), Voltage Monitor (V) and External Current Limit (X) Inputs							
Auto-Restart Hysteresis Voltage	$V_{C(AR)hyst}$			0.8	1.0		V
Auto-Restart Duty Cycle	$DC_{(AR)}$				2	4	%
Auto-Restart Frequency	$f_{(AR)}$				0.5		Hz
Line Undervoltage Threshold Current and Hysteresis (M or V Pin)	I_{UV}	T_J = 25 °C	Threshold	22	25	27	µA
			Hysteresis		14		µA
Line Overvoltage Threshold Current and Hysteresis (M or V Pin)	I_{OV}	T_J = 25 °C	Threshold	107	112	117	µA
			Hysteresis		4		µA

TO-220-7C







Y07C MOUNTING HOLE PATTERN

Notes:

1. Controlling dimensions are inches. Millimeter dimensions are shown in parentheses.
2. Pin numbers start with Pin 1, and continue from left to right when viewed from the front.
3. Dimensions do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15mm) on any side.
4. Minimum metal to metal spacing at the package body for omitted pin locations is .068 in. (1.73 mm).
5. Position of terminals to be measured at a location .25 (6.35) below the package body.
6. All terminals are solder plated.

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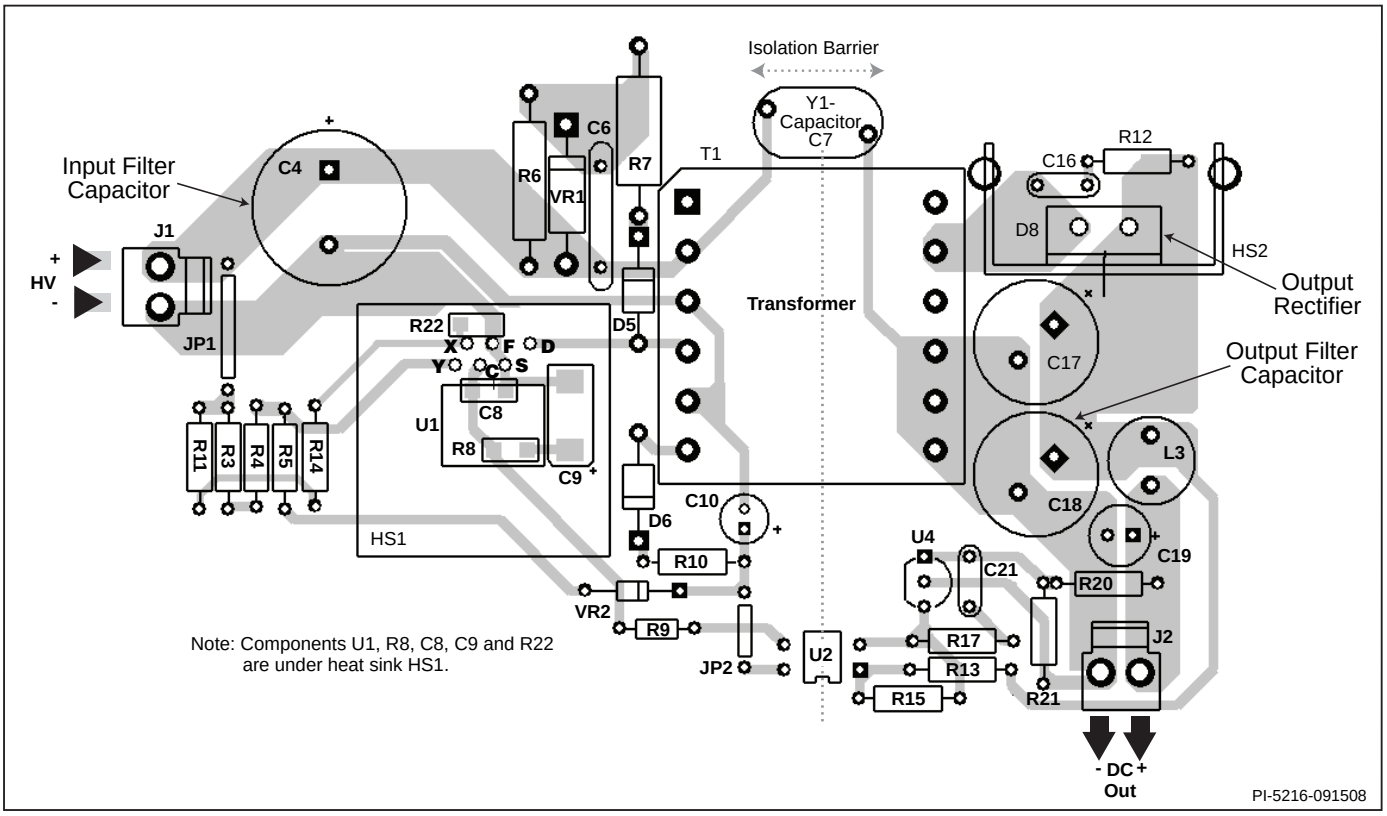

Figure 50c. Layout Considerations for TOPSwitch-HX Using L Package and Operating at 132 kHz.

Quick Design Checklist

In order to reduce the no-load input power of TOPSwitch-HX designs, the X-pin (or X-pin for P PacXage) operates at very low currentX This requires careful layout considerations when designing the PCX to avoid noise couplingX Traces and components connected to the X-pin should not Xe adXacent to any traces carrying switching currentsX These include the drain, clamp networX, Xias winding return or power traces from other convertersX If the line sensing features are used, then the sense resistors must Xe placed within XX mm of the X-pin to minimize the X pin node areaX The XC Xus should then Xe routed to the line sense resistorsX XXote that external capacitance must not Xe connected to the X-pin as this may cause misoperation of the X pin related functionsX

As with any power supply design, all TOPSwitch-HX designs should Xe verieX on the Xench to maXe sure that components speciXications are not exceeded under worst-case conditionsX The following minimum set of tests is strongly recommendedX

XX XaximXm drain voltage X XerifX that peaX X$_{XS}$ does not exceed XXX X at highest input voltage and maximum overload output powerX XaximXm overload output power occXrs when the output is overloaded to a level XXst Xefore the power sXpply goes into aXto-restart (loss of regXlation)X

XX XaximXm drain cXrrent X At maximXm amXient temperatXre, maximXm input voltage and maximXm otXpXt load, verify drain cXrrent waveforms at start-Xp for any signs of trans-former saXration and excessive leading edge cXrrent spiXes X TOPSwitch-HX has a leading edge XlanXing time of XXX ns to prevent premature termination of the OX-cycleX XerifX that the leading edge cXrrent spiXe is Xelow the allowed cXrrent limit envelope (see Figure XX) for the drain cXrrent waveform at the end of the XXX ns XlanXing periodX

XX Thermal checX X At maximXm otXpXt power, Xoth minimXm and maximXm voltage and amXient temperatXre, verifX that temperatXre speciXications are not exceeded for TOPSwitch-HX, transformer, otXpXt diodes and otXpXt capacitorsX Enogh thermal margin should Xe allowed for the part-to-part variation of the R$_{XS(OX)}$ of TOPSwitch-HX, as speciXed in the data sheetX The margin reqXired can either Xe calcXlated from the values in the parameter taXle or it can Xe accoXnted for Xy connecting an external resistance in series with the XRAIX pin and attached to the same heat sinX, having a resistance valXe that is eqXal to the difference Xetween the measXred R$_{XS(OX)}$ of the device Xnder test and the worst case maximXm speciXicationX

Design Tools

XpXto-date information on design tools can Xe fonnd at the Power Integrations weXsiteX wwwXpowerintXcom

Absolute Maximum Ratings [2]

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□□ □aximum ratings speci□ed may □e applied one at a time without causing permanent damage to the product□ Exposure to A□solute □aximum Rating conditions for extended periods of time may affect product relia□ility□

Thermal Impedance

Thermal Impedance□ □ Pac□age□
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□□ Soldered to □ sq□ in□ (□□□ mm[□]), □ oz□ (□□□ g□m[□]) copper clad□
□□ □easured on the SO□RCE pin close to plastic interface□

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 54 (Unless Otherwise Speci ed)		Min	Typ	Max	Units
Control Functions							
Switching Frequency in Full Frequency Mode (average)	f_{OSC}	T_J □ □□ □C	FREQ□E□C□ Pin Connected to SO□RCE TOP□□□-□□□□ TOP□□□-□□□L TOP□□□-□□□E	□□□	□□□	□□□	□Hz
			FREQ□E□C□ Pin Connected to CO□TROL TOP□□□-□□□□ TOP□□□-□□□L TOP□□□-□□□E	□□□□	□□	□□□□	
			TOP□□□-□□□P□G□□ TOP□□□-□□□□	□□□□	□□	□□□□	
Frequency Jitter Deviation	Δf		□□□ □Hz Operation		□		□Hz
			□□ □Hz Operation		□□□		
Frequency Jitter Modulation Rate	$f_□$				□□□		Hz
Maximum Duty Cycle	$□C_{□A□}$	I_C □ $I_{C□□}$	$I_□$ □ $I_{□(□C)}$ or $I_□$ □ $I_{□(□C)}$ or □□, □□ □ □ □	□□	□□	□□	□
			$I_□$ or $I_□$ □ □□ +A	□□			
Soft-Start Time	t_{SOFT}	T_J □ □□ □C			□□		ms
PWM Gain	$□C_{reg}$	T_J □ □□ □C	TOP□□□-□□□	-□□	-□□	-□□	□□mA
			TOP□□□-□□□	-□□	-□□	-□□	
			TOP□□□-□□□	-□□	-□□	-□□	
PWM Gain Temperature Drift		See □ote A			-□□□□		□□mA□□C
External Bias Current	$I_□$	□□ □Hz Operation	TOP□□□-□□□	□□□	□□□	□□□	mA
			TOP□□□-□□□	□□□	□□□	□□□	
			TOP□□□-□□□	□□□	□□□	□□□	

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C (Unless Otherwise Speci ed)		Min	Typ	Max	Units
Control Functions (cont.)							
External Bias Current	$I_{\square}$	□□□ □Hz Operation	TOP□□□-□□□	□□□	□□□	□□□	mA
			TOP□□□-□□□	□□□	□□□	□□□	
			TOP□□□-□□□	□□□	□□□	□□□	
CONTROL Current at 0% Duty Cycle	$I_{C(OFF)}$	□□ □Hz Operation	TOP□□□-□□□		□□□	□□□	mA
			TOP□□□-□□□		□□□	□□□	
			TOP□□□-□□□		□□□	□□□	
		□□□ □Hz Operation	TOP□□□-□□□		□□□	□□□	
			TOP□□□-□□□		□□□	□□□	
			TOP□□□-□□□		□□□	□□□	
Dynamic Impedance	$□_C$	I_C □ □ mA□ T_J □ □□ □C, See Figure □□		□□	□□	□□	1
Dynamic Impedance Temperature Drift					□□□		□□□C
CONTROL Pin Internal Filter Pole					□		□Hz
Upper Peak Current to Set Current Limit Ratio	$□_{PS(□PPER)}$	T_J □ □□ □C See □ote □		□□	□□	□□	□
Lower Peak Current to Set Current Limit Ratio	$□_{PS(LOWER)}$	T_J □ □□ □C See □ote □			□□		□
Multi-Cycle-Modulation Switching Frequency	$f_{□C□(□□□)}$	T_J □ □□ □C			□□		□Hz
Minimum Multi-Cycle-Modulation On Period	$T_{□C□(□□□)}$	T_J □ □□ □C			□□□		-s
Shutdown/Auto-Restart							
Control Pin Charging Current	$I_{C(CH)}$	T_J □ □□ □C	$□_C$ □ □ □	-□□□	-□□□	-□□□	mA
			$□_C$ □ □ □	-□□□	-□□□	-□□□	
Charging Current Temperature Drift		See □ote A			□□□		□□□C
Auto-Restart Upper Threshold Voltage	$□_{C(AR)□}$				□□□		□
Auto-Restart Lower Threshold Voltage	$□_{C(AR)L}$			□□□	□□□	□□□	□
Multi-Function (M), Voltage Monitor (V) and External Current Limit (X) Inputs							
Auto-Restart Hysteresis Voltage	$□_{C(AR)hyst}$			□□□	□□□		□
Auto-Restart Duty Cycle	□C $_{(AR)}$				□	□	□
Auto-Restart Frequency	$f_{(AR)}$				□□□		Hz
Line Undervoltage Threshold Current and Hysteresis (M or V Pin)	$I_{□□}$	T_J □ □□ □C	Threshold	□□	□□	□□	-A
			Hysteresis		□□		-A
Line Overvoltage Threshold Current and Hysteresis (M or V Pin)	$I_{O□}$	T_J □ □□ □C	Threshold	□□□	□□□	□□□	-A
			Hysteresis		□		-A

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Multi-Function (M), Voltage Monitor (V) and External Current Limit (X) Inputs							
Output Overvoltage Latching Shutdown Threshold Current	$I_{O(LS)}$	T_J = 25 °C		450	500	550	µA
V or M Pin Reset Voltage	$V_{(TH)}$ or $V_{(TH)}$	T_J = 25 °C		1.20	1.25	1.30	V
Remote ON/OFF Negative Threshold Current and Hysteresis (M or X Pin)	$I_{REM(N)}$	T_J = 25 °C	Threshold	-80	-100	-120	µA
			Hysteresis		8		
V or M Pin Short Circuit Current	$I_{(SC)}$ or $I_{(SC)}$	T_J = 25 °C	$V_{(TH)}$, $V_{(TH)}$ = 0 V	450	500	550	µA
X or M Pin Short Circuit Current	$I_{(SC)}$ or $I_{(SC)}$	$V_{(TH)}$, $V_{(TH)}$ = 0 V	Normal Mode	-450	-500	-550	µA
			Auto-Restart Mode	-80	-100	-120	
V or M Pin Voltage (Positive Current)	$V_{(TH)}$ or $V_{(TH)}$		$I_{(TH)}$ or $I_{(TH)}$ = $I_{(SC)}$	1.20	1.25	1.30	V
		$I_{(TH)}$ or $I_{(TH)}$ = $I_{O(LS)}$	TOPX00-TOPX00	1.20	1.25	1.30	
			TOPX00-TOPX00	1.20	1.25	1.30	
V or M Pin Voltage Hysteresis (Positive Current)	$V_{(TH)(hyst)}$ or $V_{(TH)(hyst)}$		$I_{(TH)}$ or $I_{(TH)}$ = $I_{O(LS)}$	0.05	0.08		V
X or M Pin Voltage (Negative Current)	$V_{(TH)}$ or $V_{(TH)}$		$I_{(TH)}$ or $I_{(TH)}$ = -100 µA	1.20	1.25	1.30	V
			$I_{(TH)}$ or $I_{(TH)}$ = -200 µA	1.20	1.25	1.30	
Maximum Duty Cycle Reduction Onset Threshold Current	$I_{(DCR)}$ or $I_{(DCR)}$	I_C = $I_{(SC)}$, T_J = 25 °C		1.20	1.25	1.30	µA
Maximum Duty Cycle Reduction Slope		T_J = 25 °C	$I_{(DCR)}$ = $I_{(SC)}$ - 100 µA or $I_{(DCR)}$ = $I_{(SC)}$ - 200 µA		-0.005		0.01 µA
			$I_{(TH)}$ or $I_{(TH)}$ = 0 µA		-0.0125		
Remote OFF DRAIN Supply Current	$I_{D(REMOT)}$	V_{DRAIN} = 100 V	X, V or M Pin Floating		0.50	0.60	mA
			V or M Pin Shorted to CONTROL		0.50	0.60	
Remote ON Delay	$t_{R(ON)}$	From Remote OFF to Drain Turn-On See Note 8	100 kHz		0.50		µs
			132 kHz		0.50		
Remote OFF Setup Time	$t_{R(OFF)}$	Minimum Time Before Drain Turn-On to Disable Cycle See Note 8	100 kHz		0.50		µs
			132 kHz		0.50		
Frequency Input							
FREQUENCY Pin Threshold Voltage	V_F	See Note 8			0.50		V
FREQUENCY Pin Input Current	I_F	T_J = 25 °C	V_F = 0 V	90	100	110	µA

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Circuit Protection							
Self Protection Current Limit (See Note C)	$I_{\text{LI[illegible]IT}}$	TOP[illegible]P[illegible]G[illegible] T_J [illegible] [illegible] [illegible]C	di[illegible]dt [illegible] [illegible] mA[illegible]s	[illegible]	[illegible]	[illegible]	A
		TOP[illegible]E[illegible] T_J [illegible] [illegible] [illegible]C	di[illegible]dt [illegible] [illegible] mA[illegible]s	[illegible]	[illegible]	[illegible]	
		TOP[illegible]P[illegible]G[illegible] T_J [illegible] [illegible] [illegible]C	di[illegible]dt [illegible] [illegible] mA[illegible]s	[illegible]	[illegible]	[illegible]	
		TOP[illegible] T_J [illegible] [illegible] [illegible]C	di[illegible]dt [illegible] [illegible] mA[illegible]s	[illegible]	[illegible]	[illegible]	
		TOP[illegible]E[illegible] T_J [illegible] [illegible] [illegible]C	di[illegible]dt [illegible] [illegible] mA[illegible]s	[illegible]	[illegible]	[illegible]	
		TOP[illegible]P[illegible]G[illegible] T_J [illegible] [illegible] [illegible]C	di[illegible]dt [illegible] [illegible] mA[illegible]s	[illegible]	[illegible]	[illegible]	
		TOP[illegible] T_J [illegible] [illegible] [illegible]C	di[illegible]dt [illegible] [illegible] mA[illegible]s	[illegible]	[illegible]	[illegible]	
		TOP[illegible]E[illegible] T_J [illegible] [illegible] [illegible]C	di[illegible]dt [illegible] [illegible] mA[illegible]s	[illegible]	[illegible]	[illegible]	
		TOP[illegible]P[illegible]G[illegible] T_J [illegible] [illegible] [illegible]C	di[illegible]dt [illegible] [illegible] mA[illegible]s	[illegible]	[illegible]	[illegible]	
		TOP[illegible] T_J [illegible] [illegible] [illegible]C	di[illegible]dt [illegible] [illegible] mA[illegible]s	[illegible]	[illegible]	[illegible]	
		TOP[illegible]L[illegible] T_J [illegible] [illegible] [illegible]C	di[illegible]dt [illegible] [illegible] mA[illegible]s	[illegible]	[illegible]	[illegible]	
		TOP[illegible]E[illegible] T_J [illegible] [illegible] [illegible]C	di[illegible]dt [illegible] [illegible] mA[illegible]s	[illegible]	[illegible]	[illegible]	
		TOP[illegible]P[illegible]G[illegible] T_J [illegible] [illegible] [illegible]C	di[illegible]dt [illegible] [illegible] mA[illegible]s	[illegible]	[illegible]	[illegible]	
		TOP[illegible] T_J [illegible] [illegible] [illegible]C	di[illegible]dt [illegible] [illegible] mA[illegible]s	[illegible]	[illegible]	[illegible]	
		TOP[illegible]L[illegible] T_J [illegible] [illegible] [illegible]C	di[illegible]dt [illegible] [illegible] mA[illegible]s	[illegible]	[illegible]	[illegible]	
		TOP[illegible]E[illegible] T_J [illegible] [illegible] [illegible]C	di[illegible]dt [illegible] [illegible] mA[illegible]s	[illegible]	[illegible]	[illegible]	
		TOP[illegible]P[illegible]G[illegible] T_J [illegible] [illegible] [illegible]C	di[illegible]dt [illegible] [illegible] mA[illegible]s	[illegible]	[illegible]	[illegible]	
		TOP[illegible] T_J [illegible] [illegible] [illegible]C	di[illegible]dt [illegible] [illegible] mA[illegible]s	[illegible]	[illegible]	[illegible]	
		TOP[illegible]L[illegible] T_J [illegible] [illegible] [illegible]C	di[illegible]dt [illegible] [illegible] mA[illegible]s	[illegible]	[illegible]	[illegible]	
		TOP[illegible]E[illegible] T_J [illegible] [illegible] [illegible]C	di[illegible]dt [illegible] [illegible] mA[illegible]s	[illegible]	[illegible]	[illegible]	
		TOP[illegible]P[illegible]G[illegible] T_J [illegible] [illegible] [illegible]C	di[illegible]dt [illegible] [illegible] mA[illegible]s	[illegible]	[illegible]	[illegible]	
		TOP[illegible] T_J [illegible] [illegible] [illegible]C	di[illegible]dt [illegible] [illegible] mA[illegible]s	[illegible]	[illegible]	[illegible]	
		TOP[illegible]L[illegible] T_J [illegible] [illegible] [illegible]C	di[illegible]dt [illegible] [illegible] mA[illegible]s	[illegible]	[illegible]	[illegible]	

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C (Unless Otherwise Speci ed)		Min	Typ	Max	Units
Circuit Protection (cont.)							
Self Protection Current Limit (See Note C)	$I_{\text{LI⊠IT}}$	TOP⊠⊠⊠⊠⊠E⊠ T_J ⊠ ⊠⊠ ⊠C	di⊠dt ⊠ ⊠⊠⊠ mA⊠+s	⊠⊠⊠⊠⊠	⊠⊠⊠⊠	⊠⊠⊠⊠⊠	A
		TOP⊠⊠⊠L⊠ T_J ⊠ ⊠⊠ ⊠C	di⊠dt ⊠ ⊠⊠⊠ mA⊠+s	⊠⊠⊠⊠⊠	⊠⊠⊠⊠	⊠⊠⊠⊠⊠	
		TOP⊠⊠⊠⊠⊠E⊠ T_J ⊠ ⊠⊠ ⊠C	di⊠dt ⊠ ⊠⊠⊠⊠ mA⊠+s	⊠⊠⊠⊠⊠	⊠⊠⊠⊠	⊠⊠⊠⊠⊠	
		TOP⊠⊠⊠L⊠ T_J ⊠ ⊠⊠ ⊠C	di⊠dt ⊠ ⊠⊠⊠ mA⊠+s	⊠⊠⊠⊠⊠	⊠⊠⊠⊠	⊠⊠⊠⊠⊠	
		TOP⊠⊠⊠⊠⊠E⊠ T_J ⊠ ⊠⊠ ⊠C	di⊠dt ⊠ ⊠⊠⊠⊠ mA⊠+s	⊠⊠⊠⊠⊠	⊠⊠⊠⊠	⊠⊠⊠⊠⊠	
		TOP⊠⊠⊠L⊠ T_J ⊠ ⊠⊠ ⊠C	di⊠dt ⊠ ⊠⊠⊠⊠ mA⊠+s	⊠⊠⊠⊠⊠	⊠⊠⊠⊠	⊠⊠⊠⊠⊠	
		TOP⊠⊠⊠⊠⊠E⊠ T_J ⊠ ⊠⊠ ⊠C	di⊠dt ⊠ ⊠⊠⊠⊠ mA⊠+s	⊠⊠⊠⊠⊠	⊠⊠⊠⊠	⊠⊠⊠⊠⊠	
		TOP⊠⊠⊠L⊠ T_J ⊠ ⊠⊠ ⊠C	di⊠dt ⊠ ⊠⊠⊠⊠ mA⊠+s	⊠⊠⊠⊠⊠	⊠⊠⊠⊠	⊠⊠⊠⊠⊠	
		TOP⊠⊠⊠E⊠ T_J ⊠ ⊠⊠ ⊠C	di⊠dt ⊠ ⊠⊠⊠⊠ mA⊠+s	⊠⊠⊠⊠⊠	⊠⊠⊠⊠	⊠⊠⊠⊠⊠	
Initial Current Limit	$I_{\text{I⊠IT}}$	See ⊠ote ⊠		⊠⊠⊠⊠ ⊠ $I_{\text{LI⊠IT(⊠I⊠)}}$			A
Power Coef cient	P_{COEFF}	T_J ⊠ ⊠⊠ ⊠C, See ⊠ote ⊠	$I_⊠$ or $I_⊠$ ⊠+ ⊠⊠⊠ +A	⊠⊠⊠ ⊠ I⊠f	I⊠f	⊠⊠⊠ ⊠ I⊠f	A⊠⊠Hz
			$I_⊠$ or $I_⊠$ ⊠+ ⊠⊠⊠ +A	⊠⊠⊠ ⊠ I⊠f	I⊠f	⊠⊠⊠ ⊠ I⊠f	
Leading Edge Blanking Time	$t_{\text{LE⊠}}$	T_J ⊠ ⊠⊠ ⊠C, See Figure ⊠⊠			⊠⊠⊠		ns
Current Limit Delay	$t_{\text{IL(⊠)}}$				⊠⊠⊠		ns
Thermal Shutdown Temperature				⊠⊠⊠	⊠⊠⊠	⊠⊠⊠	⊠C
Thermal Shutdown Hysteresis					⊠⊠		⊠C
Power-Up Reset Threshold Voltage	$⊠_{\text{C(RESET)}}$	Figure ⊠⊠ (S⊠ Open Condition)		⊠⊠⊠⊠	⊠⊠⊠	⊠⊠⊠⊠	⊠
Output							
ON-State Resistance	$R_{\text{⊠S(O⊠)}}$	TOP⊠⊠⊠ $I_⊠$ ⊠ ⊠⊠ mA	T_J ⊠ ⊠⊠ ⊠C		⊠⊠⊠⊠	⊠⊠⊠⊠⊠	1
			T_J ⊠ ⊠⊠⊠ ⊠C		⊠⊠⊠⊠	⊠⊠⊠⊠⊠	
		TOP⊠⊠⊠ $I_⊠$ ⊠ ⊠⊠⊠ mA	T_J ⊠ ⊠⊠ ⊠C		⊠⊠⊠	⊠⊠⊠⊠⊠	
			T_J ⊠ ⊠⊠⊠ ⊠C		⊠⊠⊠⊠	⊠⊠⊠⊠⊠	
		TOP⊠⊠⊠ $I_⊠$ ⊠ ⊠⊠⊠ mA	T_J ⊠ ⊠⊠ ⊠C		⊠⊠⊠	⊠⊠⊠⊠	
			T_J ⊠ ⊠⊠⊠ ⊠C		⊠⊠⊠⊠	⊠⊠⊠⊠	
		TOP⊠⊠⊠ $I_⊠$ ⊠ ⊠⊠⊠ mA	T_J ⊠ ⊠⊠ ⊠C		⊠⊠⊠	⊠⊠⊠⊠	
			T_J ⊠ ⊠⊠⊠ ⊠C		⊠⊠⊠	⊠⊠⊠⊠	
		TOP⊠⊠⊠ $I_⊠$ ⊠ ⊠⊠⊠ mA	T_J ⊠ ⊠⊠ ⊠C		⊠⊠⊠	⊠⊠⊠⊠	
			T_J ⊠ ⊠⊠⊠ ⊠C		⊠⊠⊠	⊠⊠⊠⊠	
		TOP⊠⊠⊠ $I_⊠$ ⊠ ⊠⊠⊠ mA	T_J ⊠ ⊠⊠ ⊠C		⊠⊠⊠	⊠⊠⊠⊠	
			T_J ⊠ ⊠⊠⊠ ⊠C		⊠⊠⊠	⊠⊠⊠⊠	
		TOP⊠⊠⊠ $I_⊠$ ⊠ ⊠⊠⊠ mA	T_J ⊠ ⊠⊠ ⊠C		⊠⊠⊠	⊠⊠⊠⊠	
			T_J ⊠ ⊠⊠⊠ ⊠C		⊠⊠⊠	⊠⊠⊠⊠	

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Output (cont.)							
ON-State Resistance	$R_{DS(ON)}$	TOP	T_J = 100 °C				1
		I_D = 0.4 A	T_J = 25 °C				
		TOP	T_J = 100 °C				
		I_D = 0.4 A	T_J = 25 °C				
		TOP	T_J = 100 °C				
		I_D = 0.4 A	T_J = 25 °C				
		TOP	T_J = 100 °C				
		I_D = 0.4 A	T_J = 25 °C				
DRAIN Supply Voltage		T_J = 100 °C, See Note E		50			V
				50			
OFF-State Drain Leakage Current	I_{DSS}	V_D, V_D = Floating, I_C = 0 mA, V_{DS} = 0.8 x $V_{(BR)DSS}$, T_J = 125 °C				50	μA
Breakdown Voltage	$V_{(BR)DSS}$	V_D, V_D = Floating, I_C = 0 mA, T_J = 25 °C See Note F		700			V
Rise Time	t_R	Measured in a Typical Flyback Converter Application			100		ns
Fall Time	t_F				50		ns
Supply Voltage Characteristics							
Control Supply/ Discharge Current	I_{CD}	Output MOSFET Enabled V_D, V_D, V_D = 0 V	50 kHz Operation	TOP			mA
				TOP			
				TOP			
			100 kHz Operation	TOP			
				TOP			
				TOP			
	I_{CD}	Output MOSFET Disabled V_D, V_D, V_D = 0 V					

NOTES:

A. For specifications with negative values, a negative temperature coefficient corresponds to an increase in magnitude with increasing temperature, and a positive temperature coefficient corresponds to a decrease in magnitude with increasing temperature.

B. Guaranteed by characterization. Not tested in production.

C. For externally adjusted current limit values, please refer to Figures 10a and 10b (Current Limit vs. External Current Limit Resistance) in the Typical Performance Characteristics section. The tolerance specified is only valid at full current limit.

D. If calculation is based on typical values of f_{LIMIT} and f_{OSC}, i.e. $I_{LIMIT(TYP)} = I_{LIMIT} \times f_{OSC}$, where f_{OSC} = 100 kHz or 132 kHz depending on package F pin connection. See f_{OSC} specification for detail.

E. The TOPSwitch-HX will start up at 50 V V_C drain voltage. The capacitance of electrolytic capacitors drops significantly at temperatures below 0 °C. For reliable start up at 50 V in sub zero temperatures, designers must ensure that circuit capacitors meet recommended capacitance values.

F. Breakdown voltage may be checked against minimum $V_{(BR)DSS}$ specification by ramping the BPAI pin voltage up to but not exceeding minimum $V_{(BR)DSS}$.

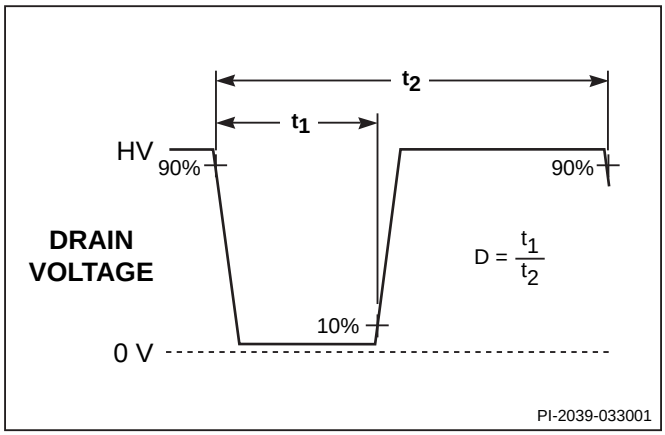

Figure 51. Duty Cycle Measurement.

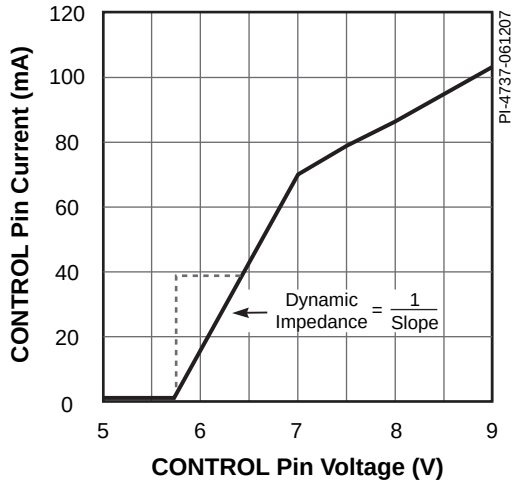

Figure 52. CONTROL Pin I-V Characteristic.

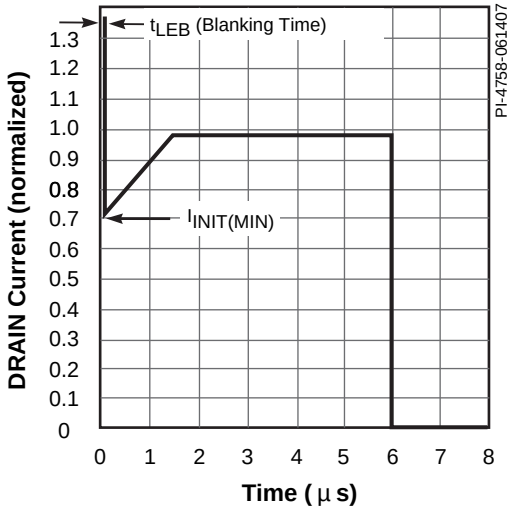

Figure 53. Drain Current Operating Envelope.

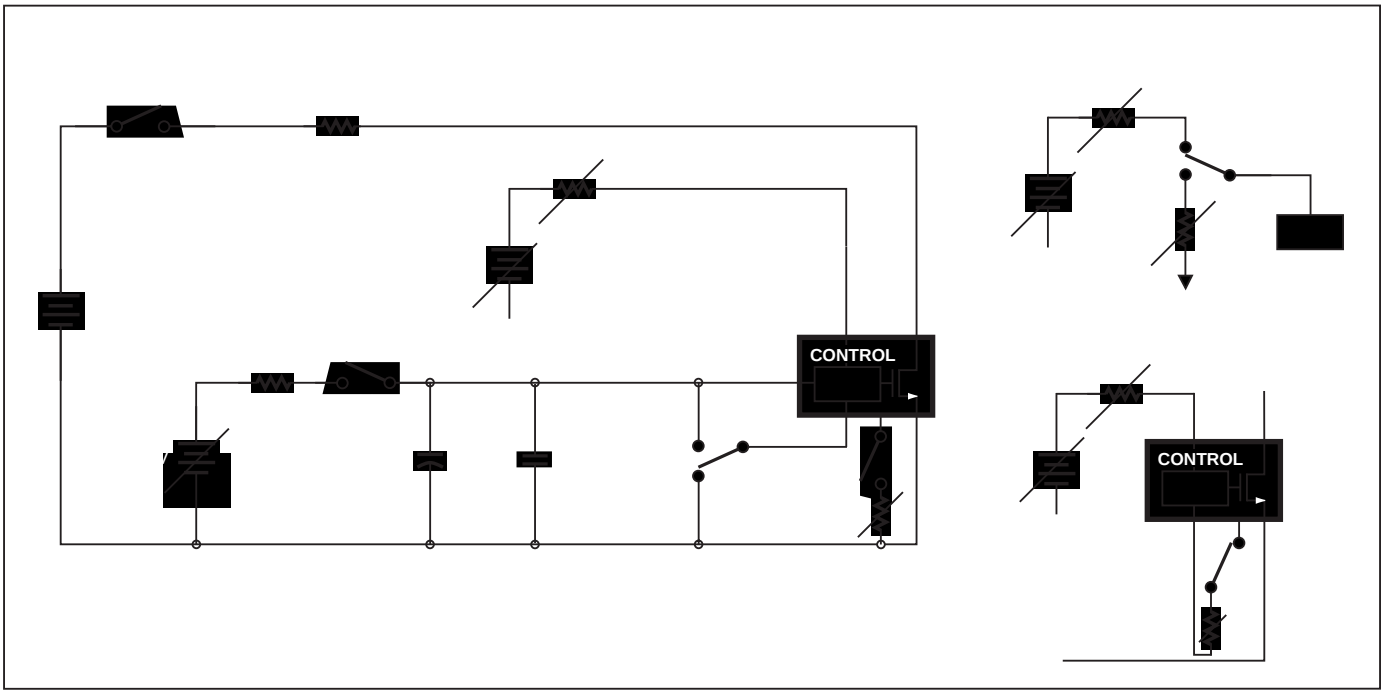

Figure 54. TOPSwitch-HX General Test Circuit.

Typical Performance Characteristics

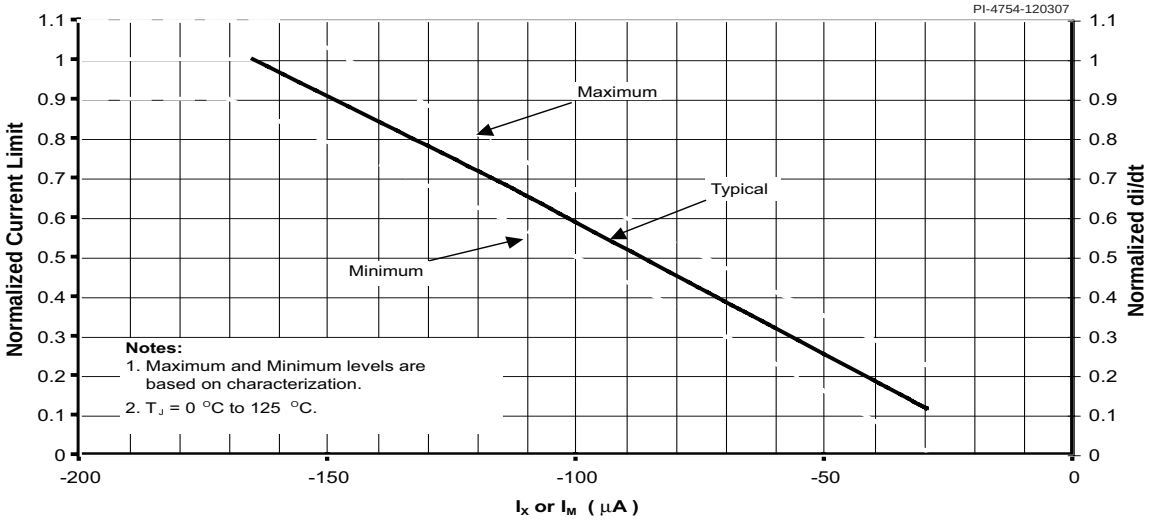

Figure 55a. Normalized Current Limit vs. X or M Pin Current.

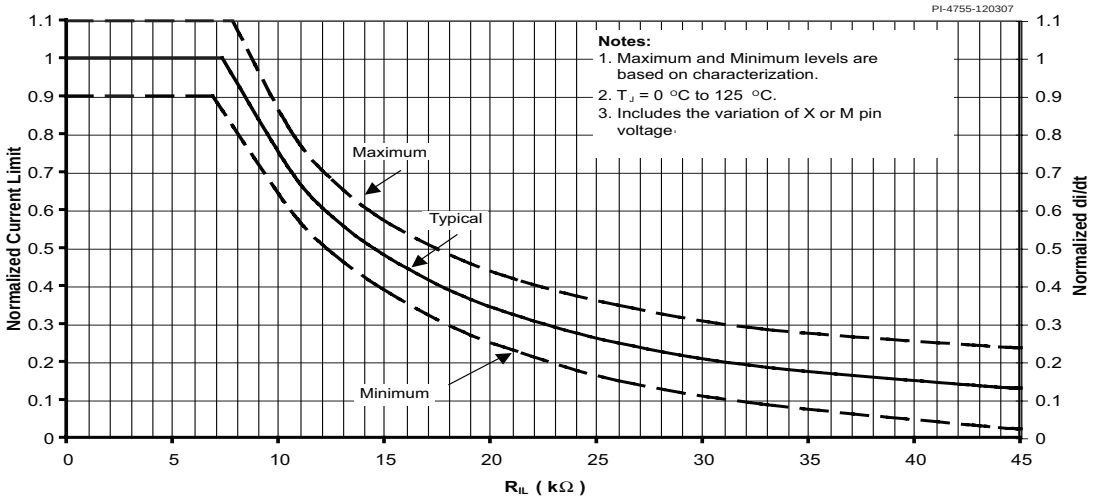

Figure 55b. Normalized Current Limit vs. External Current Limit Resistance.

Typical Performance Characteristics (cont.)

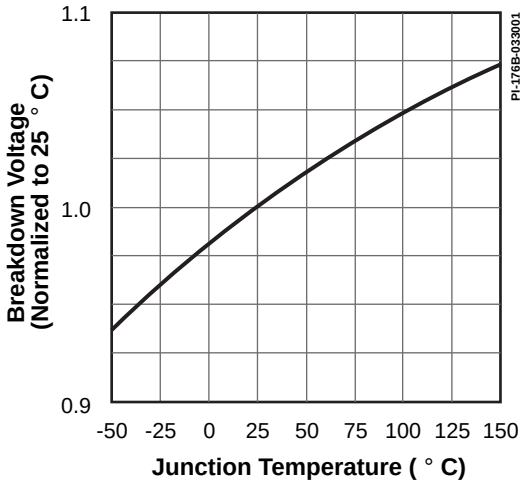

Figure 56. Breakdown Voltage vs. Temperature.

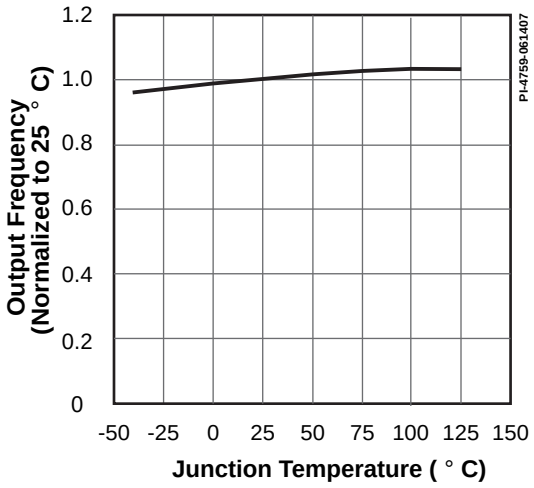

Figure 57. Frequency vs. Temperature.

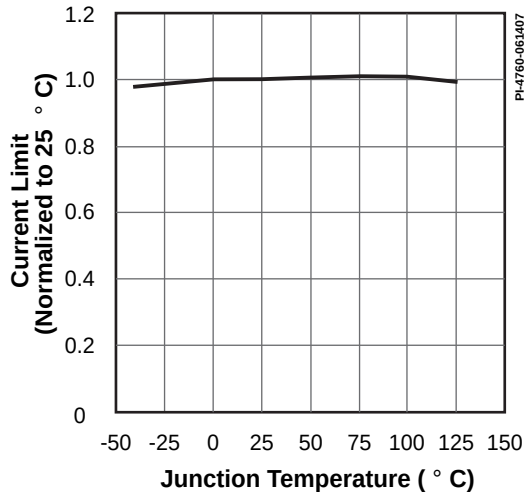

Figure 58. Internal Current Limit vs. Temperature.

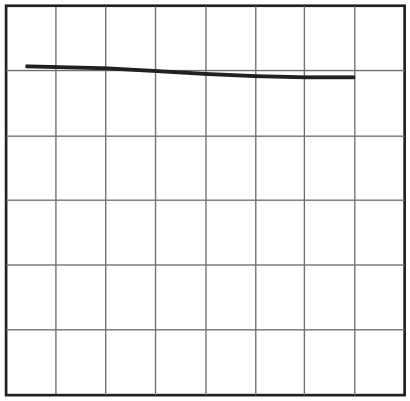

Figure 59. External Current Limit vs. Temperature with R_L= 10.5 k 1.

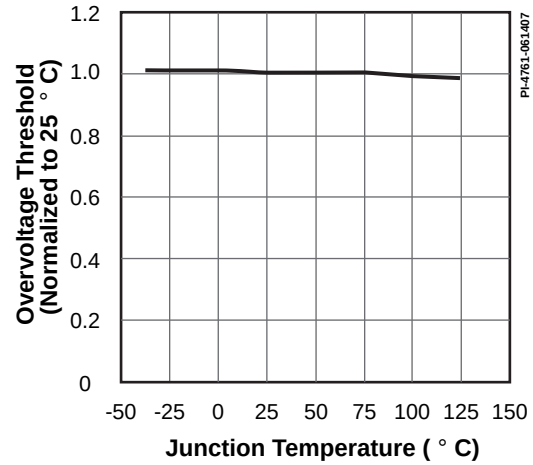

Figure 60. Overvoltage Threshold vs. Temperature.

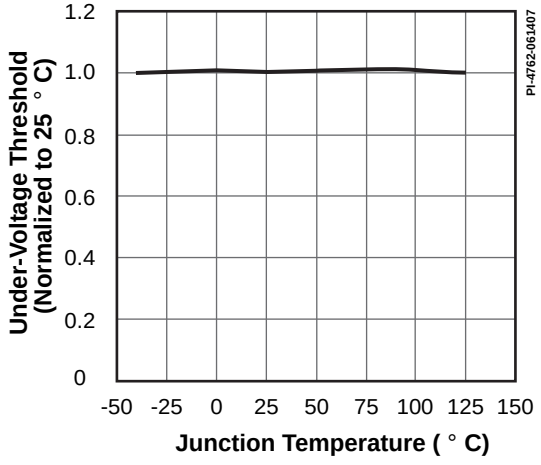

Figure 61. Undervoltage Threshold vs. Temperature.

Typical Performance Characteristics (cont.)

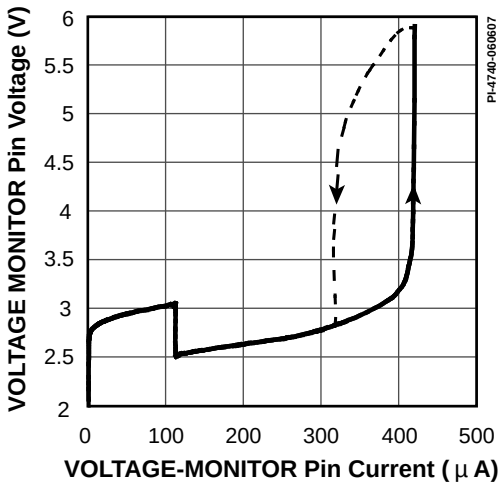

Figure 62a. VOLTAGE-MONITOR Pin vs. Current.

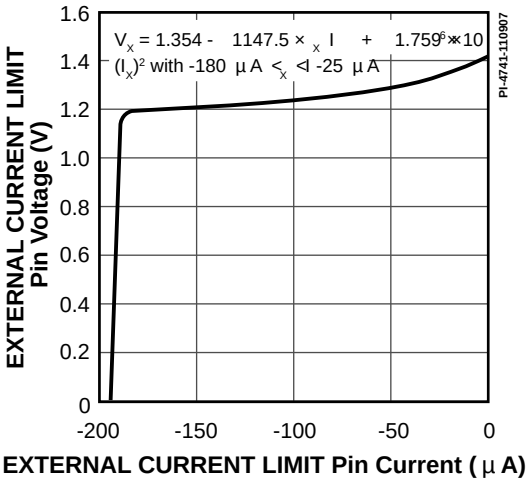

Figure 62b. EXTERNAL CURRENT LIMIT Pin Voltage vs. Current.

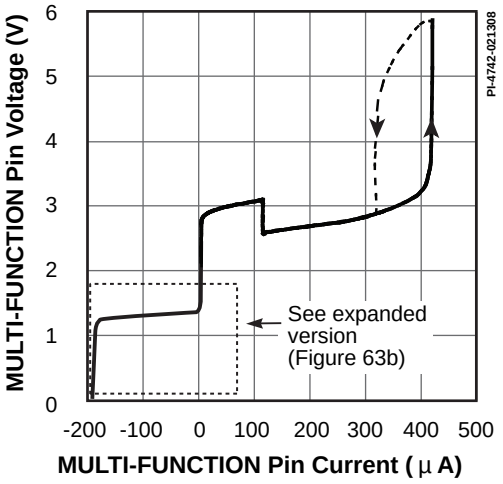

Figure 63a. MULTI-FUNCTION Pin Voltage vs. Current.

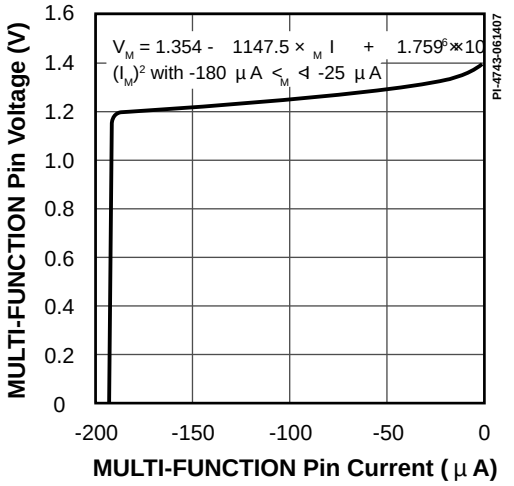

Figure 63b. MULTI-FUNCTION Pin Voltage vs. Current (Expanded).

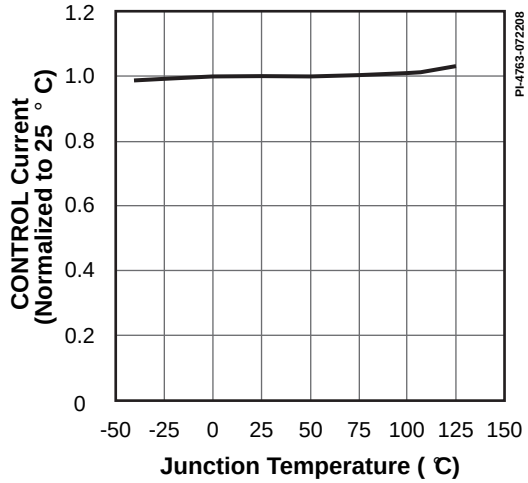

Figure 64. Control Current Out at 0% Duty Cycle vs. Temperature.

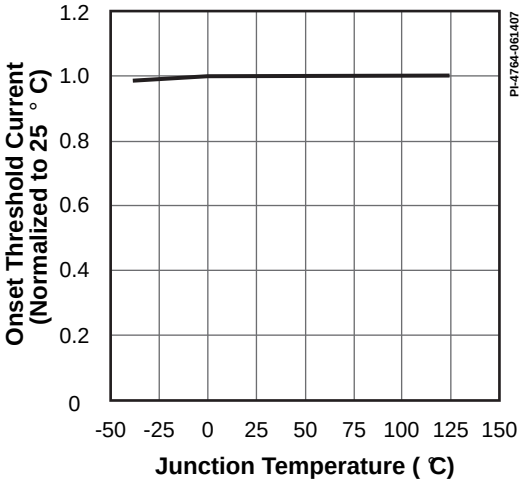

Figure 65. Maximum Duty Cycle Reduction Onset Threshold Current vs. Temperature.

Typical Performance Characteristics (cont.)

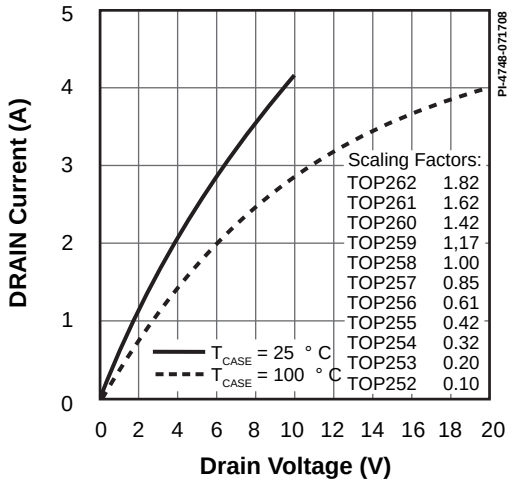

Figure 66. Output Characteristics.

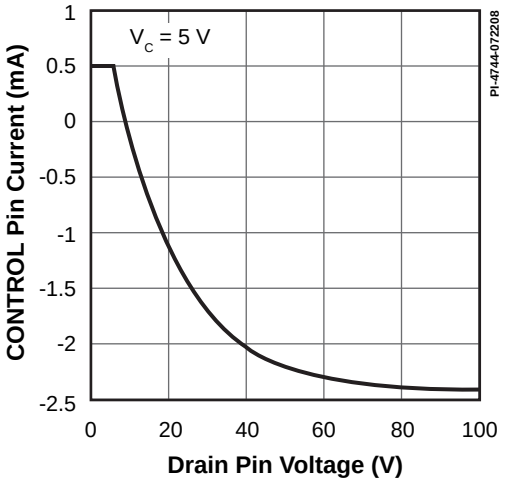

Figure 67. I_C vs. DRAIN Voltage.

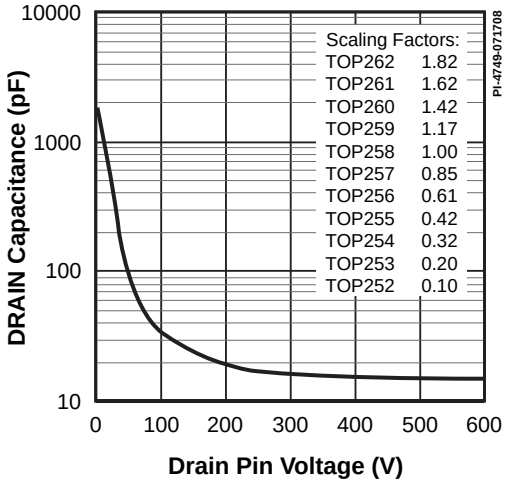

Figure 68. C_{OSS} vs. DRAIN Voltage.

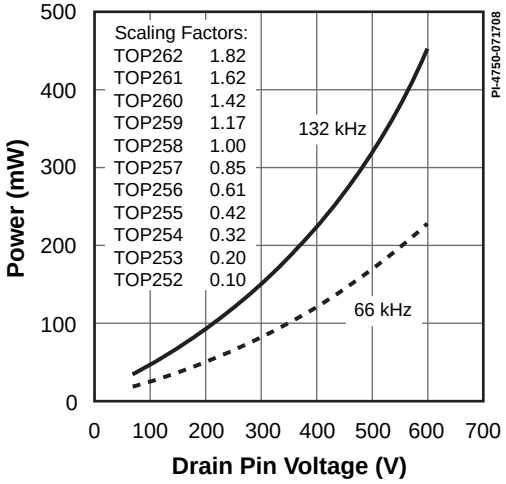

Figure 69. DRAIN Capacitance Power.

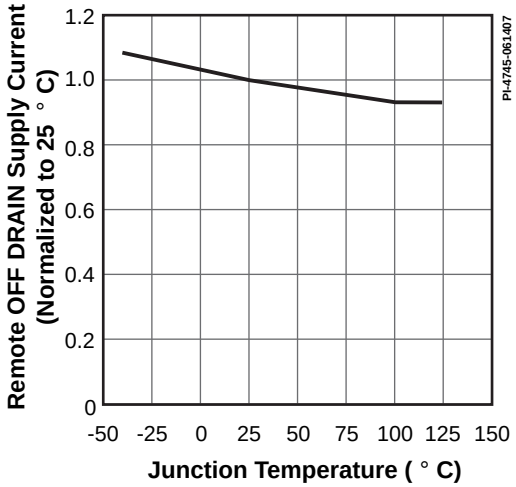

Figure 70. Remote OFF DRAIN Supply Current vs. Temperature.