TS5A3157 10-Ω SPDT Analog Switch

1 Features

- Low ON-State Resistance (10 Ω)
- Control Inputs Are 5-V Tolerant
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Sample-and-Hold Circuits
- Battery-Powered Equipment
- Audio and Video Signal Routing
- Communication Circuits

3 Description

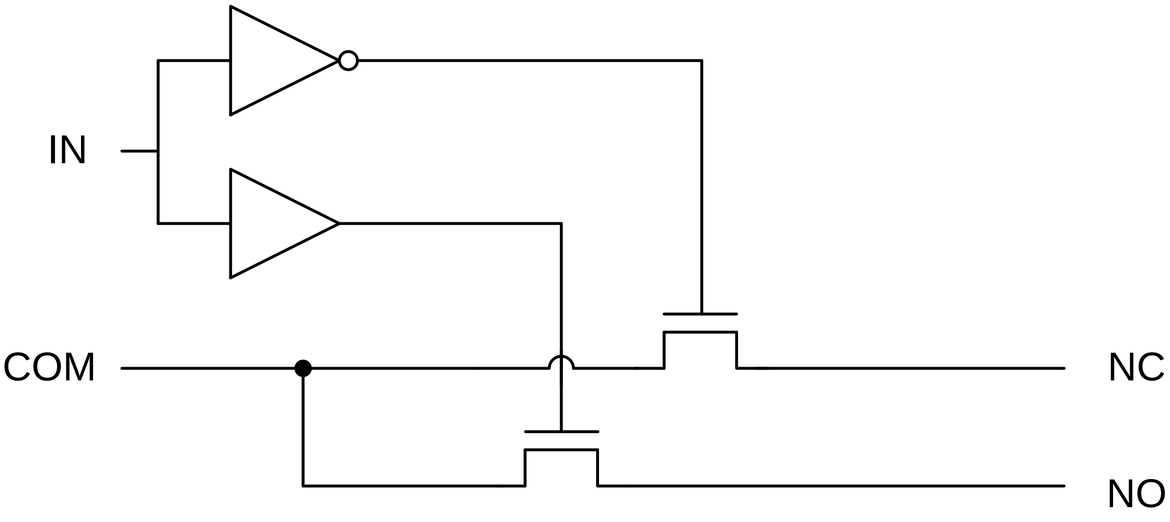
The TS5A3157 device is a single-pole double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 5.5 V. This device can handle both digital and analog signals, and signals up to V_+ can be transmitted in either direction.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS5A3157	SOT-23 (6)	2.90 mm × 1.60 mm
	SC70 (6)	2.00 mm × 1.25 mm
	DSBGA (6)	1.39 mm × 0.89 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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4 Revision History

Changes from Revision A (September 2004) to Revision B **Page**

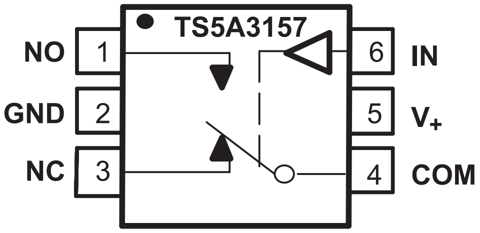
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Removed *Ordering Information* table. ... 1

Changes from Original (August 2004) to Revision A **Page**

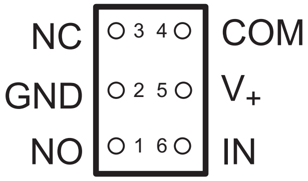
- Updated document to new TI data sheet format - no specification changes. ... 1

5 Pin Configuration and Functions

DBV and DCK Packages
6-Pin SOT-23 and SC-70
(Top View)



YZP Package
6-Pin DSBGA
(Bottom View)



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	NO	I/O	Normally open switch port
2	GND	—	Ground
3	NC	I/O	Normally closed switch port
4	COM	I/O	Common switch port
5	V+	—	Power supply
6	IN	I	Switch select. High = COM connected to NO; Low = COM connected to NC.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2]

			MIN	MAX	UNIT
V_+	Supply voltage[3]		–0.5	6.5	V
V_{NO} V_{NC} V_{COM}	Analog voltage[3][4][5]		–0.5	V_+ + 0.5	V
I_K	Analog port diode current	V_{NC}, V_{NO}, V_{COM} < 0 or V_{NO}, V_{NC}, V_{COM} > V_+	–50	50	mA
I_{NO} I_{NC} I_{COM}	On-state switch current	V_{NC}, V_{NO}, V_{COM} = 0 to V_+	–50	50	mA
V_I	Digital input voltage[3][4]		–0.5	6.5	V
I_{IK}	Digital input clamp current	V_I < 0	–50		mA
I_+	Continuous current through V_+		–100	100	mA
I_{GND}	Continuous current through GND		–100	100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Switch input/output voltage	0	V_+	V
V+	Supply voltage	1.65	5.5	V
V_I	Control input voltage	0	5.5	V
T_A	Operating temperature	–40	85	°C

6.4 Thermal Information

THERMAL METRIC[1]		TS5A3157			UNIT
		DBV (SOT-23)	DCK (SC-70)	YZP (DSBGA)	
		6 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	206	252	132	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics for 5-V Supply

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{on}	ON-state resistance	$0 \leq (V_{NO}$ or $V_{NC}) \leq V_+$, I_{COM} = –30 mA,	Switch ON, see Figure 12	25°C	4.5 V		5.5	10	Ω
				Full				12	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 3.15 V, I_{COM} = –30 mA,	Switch ON, see Figure 12	25°C	4.5 V		0.15	0.2	Ω
				Full				0.3	
$r_{on(flat)}$	ON-state resistance flatness	$0 \leq (V_{NO}$ or $V_{NC}) \leq V_+$, I_{COM} = –30 mA,	Switch ON, see Figure 12	25°C	4.5 V		4	5	Ω
				Full				6	
$I_{NO(OFF)}$, $I_{NC(OFF)}$	NO, NC OFF leakage current	V_{NO} or V_{NC} = 1 V, V_{COM} = 4.5 V, or V_{NO} or V_{NC} = 4.5 V, V_{COM} = 1 V,	Switch OFF, see Figure 13	25°C	5.5 V	–0.1	0.05	0.1	µA
				Full		–0.2	0.1	0.2	
$I_{NO(ON)}$, $I_{NC(ON)}$	NO, NC ON leakage current	V_{NO} = 1 V, V_{COM} = Open, or V_{NO} = 4.5 V, V_{COM} = Open,	Switch ON, see Figure 14	25°C	5.5 V	–0.1	0.05	0.1	µA
				Full		–0.2	0.1	0.2	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 1 V, V_{NO} or V_{NC} = Open, or V_{COM} = 4.5 V, V_{NO} or V_{NC} = Open,	Switch ON, see Figure 14	25°C	5.5 V	–0.1	0.05	0.1	µA
				Full		–0.2	0.1	0.2	
Digital Control Input (IN)									
V_{IH}	Input logic high			Full		V_+ × 0.7		5.5	V
V_{IL}	Input logic low			Full		0		V_+ × 0.3	V
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	5.5 V	–0.1	0.05	0.1	µA
				Full		–1		1	
Dynamic									
t_{ON}	Turnon time	V_{COM} = 3 V, R_L = 300 Ω,	C_L = 35 pF, see Figure 16	25°C	5 V	1	6	8.5	ns
				Full	4.5 V to 5.5 V	1		9.5	
t_{OFF}	Turnoff time	V_{COM} = 3 V, R_L = 300 Ω,	C_L = 35 pF, see Figure 16	25°C	5 V	1	3.5	6.5	ns
				Full	4.5 V to 5.5 V	1		7.5	
t_{BBM}	Break-before-make time	$V_{NC} = V_{NO} = V_+ / 2$, R_L = 50 Ω,	C_L = 35 pF, see Figure 17	25°C	5 V	1.8	2	3	ns
				Full	4.5 V to 5.5 V	1.8		3.5	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, see Figure 21	25°C	5 V		7		pC
$C_{NO(OFF)}$, $C_{NC(OFF)}$	NO, NC OFF capacitance	V_{NO} or V_{NC} = V_+ or GND,	Switch OFF, see Figure 15	25°C	5 V		5.5		pF
$C_{NO(ON)}$, $C_{NC(ON)}$	NO, NC ON capacitance	V_{NO} or V_{NC} = V_+ or GND,	Switch ON, see Figure 15	25°C	5 V		17.5		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND,	Switch ON, see Figure 15	25°C	5 V		17.5		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See Figure 15	25°C	5 V		2.8		pF

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics for 5-V Supply (continued)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
BW	Bandwidth	R_L = 50 Ω,	Switch ON, see Figure 18	25°C	5 V		300		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 10 MHz,	Switch OFF, see Figure 19	25°C	5 V		–65		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 10 MHz,	Switch ON, see Figure 20	25°C	5 V		–66		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, see Figure 22	25°C	5 V		0.01%		
Supply									
I_+	Positive supply current	V_I = V_+ or GND,	Switch ON or OFF	25°C	5.5 V		2.5	5	µA
				Full				10	

6.6 Electrical Characteristics for 3.3-V Supply

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{on}	ON-state resistance	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –24 mA,	Switch ON, see Figure 12	25°C	3 V		12	20	Ω
				Full				20	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 2.1 V, I_{COM} = –24 mA,	Switch ON, see Figure 12	25°C	3 V		0.2	0.4	Ω
				Full				0.3	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –24 mA,	Switch ON, see Figure 12	25°C	3 V		9	11	Ω
				Full				12	
$I_{NO(OFF)}$, $I_{NC(OFF)}$	NO, NC OFF leakage current	V_{NO} or V_{NC} = 1 V, V_{COM} = 3 V, or V_{NO} or V_{NC} = 3 V, V_{COM} = 1 V,	Switch OFF, see Figure 13	25°C	3.6 V	–0.1	0.05	0.1	µA
				Full		–0.2	0.1	0.2	
$I_{NO(ON)}$, $I_{NC(ON)}$	NO, NC ON leakage current	V_{NO} or V_{NC} = 1 V, V_{COM} = Open, or V_{NO} or V_{NC} = 3 V, V_{COM} = Open,	Switch ON, see Figure 14	25°C	3.6 V	–0.1	0.05	0.1	µA
				Full		–0.2	0.1	0.2	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 1 V, V_{NO} or V_{NC} = Open, or V_{COM} = 3 V, V_{NO} or V_{NC} = Open,	Switch ON, see Figure 14	25°C	3.6 V	–0.1	0.05	0.1	µA
				Full		–0.2	0.1	0.2	
Digital Control Input (IN)									
V_{IH}	Input logic high			Full		V_+ × 0.7		5.5	V
V_{IL}	Input logic low			Full		0		V_+ × 0.3	V
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	3.6 V	–0.1	0.05	0.1	µA
				Full		–1		1	
Dynamic									
t_{ON}	Turnon time	V_{COM} = 2 V, R_L = 300 Ω,	C_L = 35 pF, see Figure 16	25°C	3.3 V	3.5	7	9.5	ns
				Full	3 V to 3.6 V	1.5		10.5	

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(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics for 3.3-V Supply (continued)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
t_{OFF}	Turnoff time	V_{COM} = 2 V, R_L = 300 Ω,	C_L = 35 pF, see Figure 16	25°C	3.3 V	1	3.5	6.5	ns
				Full	3 V to 3.6 V	1		7.5	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+ / 2, R_L = 50 Ω,	C_L = 35 pF, see Figure 17	25°C	3.3 V	2.5	3	5	ns
				Full	3 V to 3.6 V	2		5	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, see Figure 21	25°C	3.3 V		3		pC
$C_{NO(OFF)}$	NO, NC OFF capacitance	V_{NO} or V_{NC} = V_+ or GND,	Switch OFF, see Figure 15	25°C	3.3 V		5.5		pF
$C_{NO(ON)}$	NO, NC ON capacitance	V_{NO} or V_{NC} = V_+ or GND,	Switch ON, see Figure 15	25°C	3.3 V		17.5		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND,	Switch ON, see Figure 15	25°C	3.3 V		17.5		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See Figure 15	25°C	3.3 V		2.8		pF
BW	Bandwidth	R_L = 50 Ω,	Switch ON, see Figure 18	25°C	3.3 V		300		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 10 MHz,	Switch OFF, see Figure 19	25°C	3.3 V		–65		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 10 MHz,	Switch ON, see Figure 20	25°C	3.3 V		–66		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, see Figure 22	25°C	3.3 V		0.015 %		
Supply									
I_+	Positive supply current	V_I = V_+ or GND,	Switch ON or OFF	25°C	3.6 V		2.5	5	µA
				Full			10		

6.7 Electrical Characteristics for 2.5-V Supply

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{on}	ON-state resistance	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –8 mA,	Switch ON, see Figure 12	25°C	2.3 V		35	45	Ω
				Full				50	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 1.6 V, I_{COM} = –8 mA,	Switch ON, see Figure 12	25°C	2.3 V		0.3	0.5	Ω
				Full				0.7	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –8 mA,	Switch ON, see Figure 12	25°C	2.3 V		30	40	Ω
				Full				40	
$I_{NO(OFF)}$, $I_{NC(OFF)}$	NO, NC OFF leakage current	V_{NO} or V_{NC} = 0.5 V, V_{COM} = 2.2 V, or V_{NO} or V_{NC} = 2.2 V, V_{COM} = 0.5 V,	Switch OFF, see Figure 13	25°C	2.7 V	–0.1	0.05	0.1	µA
				Full		–0.2	0.1	0.2	

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(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics for 2.5-V Supply (continued)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
$I_{NO(ON)}$, $I_{NC(ON)}$	NO, NC ON leakage current	V_{NO} or V_{NC} = 0.5 V, V_{COM} = Open, or V_{NO} or V_{NC} = 2.2 V, V_{COM} = Open,	Switch ON, see Figure 14	25°C	2.7 V	–0.1	0.05	0.1	µA
				Full		–0.2	0.1	0.2	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 0.5 V, V_{NO} or V_{NC} = Open, or V_{COM} = 2.2 V, V_{NO} or V_{NC} = Open,	Switch ON, see Figure 14	25°C	2.7 V	–0.1	0.05	0.1	µA
				Full		–0.2	0.1	0.2	
Digital Control Input (IN)									
V_{IH}	Input logic high			Full		V_+ × 0.7		5.5	V
V_{IL}	Input logic low			Full		0		V_+ × 0.3	V
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	2.7 V	–0.1	0.05	0.1	µA
				Full		–1		1	
Dynamic									
t_{ON}	Turnon time	V_{COM} = 1.5 V, R_L = 300 Ω,	C_L = 35 pF, see Figure 16	25°C	2.5 V	5	8	13.5	ns
				Full	2.3 V to 2.7 V	3.5		14	
t_{OFF}	Turnoff time	V_{COM} = 1.5 V, R_L = 300 Ω,	C_L = 35 pF, see Figure 16	25°C	2.5 V	1	3.5	6.5	ns
				Full	2.3 V to 2.7 V	1		7.5	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+ / 2, R_L = 50 Ω,	C_L = 35 pF, see Figure 17	25°C	2.5 V	3.5	5	7	ns
				Full	2.3 V to 2.7 V	3		7.5	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, see Figure 21	25°C	2.5 V		2		pC
$C_{NO(OFF)}$, $C_{NC(OFF)}$	NO, NC OFF capacitance	V_{NO} or V_{NC} = V_+ or GND,	Switch OFF, see Figure 15	25°C	2.5 V		5.5		pF
$C_{NO(ON)}$, $C_{NC(ON)}$	NO, NC ON capacitance	V_{NO} or V_{NC} = V_+ or GND,	Switch ON, see Figure 15	25°C	2.5 V		17.5		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND,	Switch ON, see Figure 15	25°C	2.5 V		17.5		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See Figure 15	25°C	2.5 V		2.8		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	2.5 V		300		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 10 MHz,	Switch OFF, see Figure 19	25°C	2.5 V		–65		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 10 MHz,	Switch ON, see Figure 20	25°C	2.5 V		–66		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, see Figure 22	25°C	2.5 V		0.025 %		
Supply									
I_+	Positive supply current	V_I = V_+ or GND,	Switch ON or OFF	25°C	2.7 V		2.5	5	µA
				Full			10		

6.8 Electrical Characteristics for 1.8-V Supply

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{on}	ON-state resistance	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –4 mA,	Switch ON, see Figure 12	25°C	1.65 V		140	160	Ω
				Full				160	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 1.16 V, I_{COM} = –4 mA,	Switch ON, see Figure 12	25°C	1.65 V		0.5	0.6	Ω
				Full				0.75	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –4 mA,	Switch ON, see Figure 12	25°C	1.65 V		125	130	Ω
				Full				140	
$I_{NO(OFF)}$, $I_{NC(OFF)}$	NO, NC OFF leakage current	V_{NO} or V_{NC} = 0.3 V, V_{COM} = 1.65 V, or V_{NO} or V_{NC} = 1.65 V, V_{COM} = 0.3 V,	Switch OFF, see Figure 13	25°C	1.95 V	–0.1	0.05	0.1	µA
				Full		–0.2	0.1	0.2	
$I_{NO(ON)}$, $I_{NC(ON)}$	NO, NC ON leakage current	V_{NO} or V_{NC} = 0.3 V, V_{COM} = Open, or V_{NO} or V_{NC} = 1.65 V, V_{COM} = Open,	Switch ON, see Figure 14	25°C	1.95 V	–0.1	0.05	0.1	µA
				Full		–0.2	0.1	0.2	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 0.3 V, V_{NO} or V_{NC} = Open, or V_{COM} = 1.65 V, V_{NO} or V_{NC} = Open,	Switch ON, see Figure 14	25°C	1.95 V	–0.1	0.05	0.1	µA
				Full		–0.2	0.1	0.2	
Digital Control Input (IN)									
V_{IH}	Input logic high			Full		V_+ × 0.65		5.5	V
V_{IL}	Input logic low			Full		0		V_+ × 0.35	V
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	1.95 V	–0.1	0.05	0.1	µA
				Full		–1		1	
Dynamic									
t_{ON}	Turnon time	V_{COM} = 1.3 V, R_L = 300 Ω,	C_L = 35 pF, see Figure 16	25°C	1.8 V	5	15	23	ns
				Full	1.65 V to 1.95 V	7		24	
t_{OFF}	Turnoff time	V_{COM} = 1.3 V, R_L = 300 Ω,	C_L = 35 pF, see Figure 16	25°C	1.8 V	1	3.5	6.5	ns
				Full	1.65 V to 1.95 V	1		7.5	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+ / 2, R_L = 50 Ω,	C_L = 35 pF, see Figure 17	25°C	1.8 V	5.5	7.5	9	ns
				Full	1.65 V to 1.95 V	5.2		12	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, see Figure 21	25°C	1.8 V		1		pC
$C_{NO(OFF)}$, $C_{NC(OFF)}$	NO, NC OFF capacitance	V_{NO} or V_{NC} = V_+ or GND,	Switch OFF, see Figure 15	25°C	1.8 V		5.5		pF
$C_{NO(ON)}$, $C_{NC(ON)}$	NO, NC ON capacitance	V_{NO} or V_{NC} = V_+ or GND,	Switch ON, see Figure 15	25°C	1.8 V		17.5		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND,	Switch ON, see Figure 15	25°C	1.8 V		17.5		pF

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics for 1.8-V Supply (continued)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
C_I	Digital input capacitance	V_I = V_+ or GND,	See Figure 15	25°C	1.8 V		2.8		pF
BW	Bandwidth	R_L = 50 Ω,	Switch ON, see Figure 18	25°C	1.8 V		300		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 10 MHz,	Switch OFF, see Figure 19	25°C	1.8 V		–65		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 10 MHz,	Switch ON, see Figure 20	25°C	1.8 V		–66		dB
THD	Total harmonic distortion	R_L = 10 kΩ, C_L = 50 pF,	f = 20 Hz to 20 kHz, see Figure 22	25°C	1.8 V		0.015 %		
Supply									
I_+	Positive supply current	V_I = V_+ or GND,	Switch ON or OFF	25°C	1.95 V		2.5	5	µA
				Full			10		

6.9 Typical Characteristics

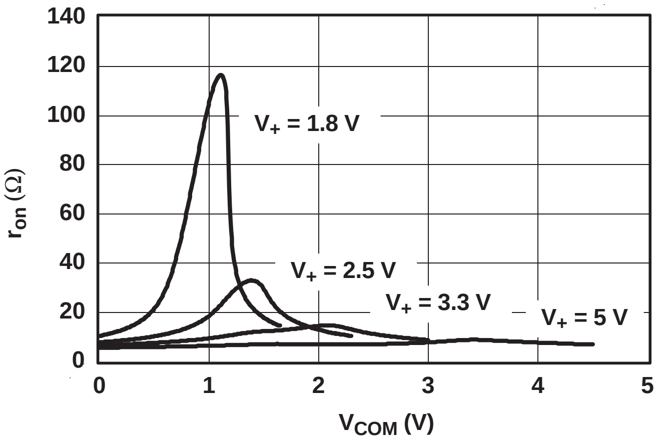


Figure 1. r_{on} vs V_{COM}

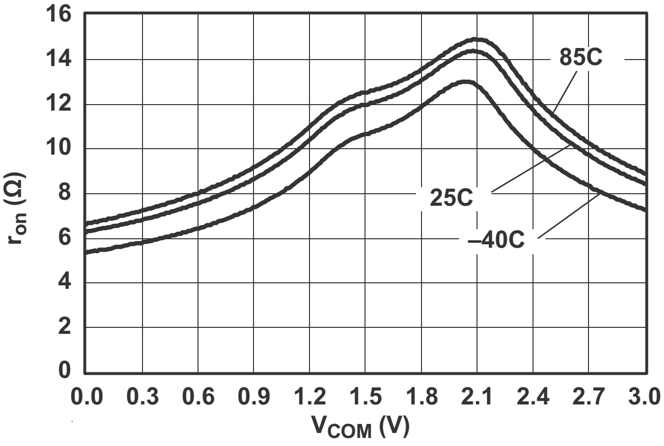


Figure 2. r_{on} vs V_{COM} (V_+ = 3 V)

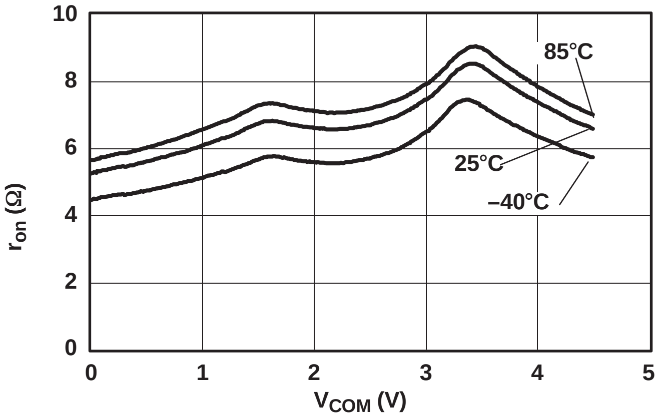


Figure 3. r_{on} vs V_{COM} (V_+ = 4.5 V)

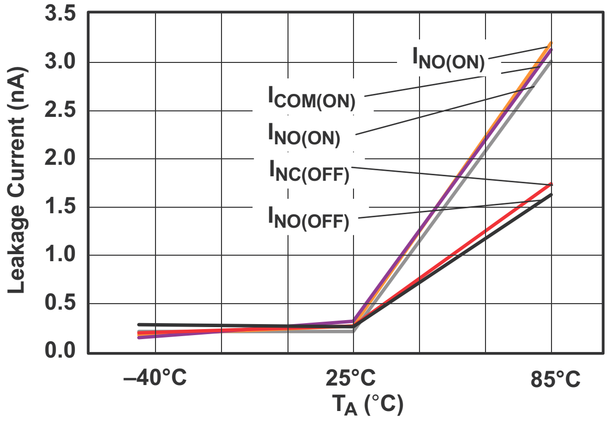


Figure 4. Leakage Current vs Temperature (V_+ = 5.5 V)

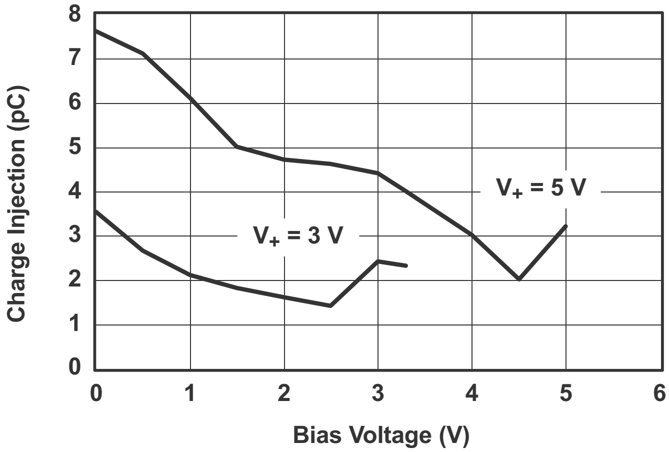


Figure 5. Charge Injection (Q_C) vs V_{COM}

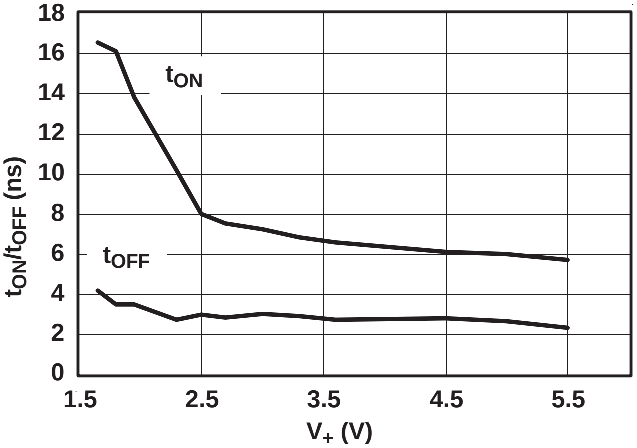


Figure 6. t_{ON} and t_{OFF} vs Supply Voltage

Typical Characteristics (continued)

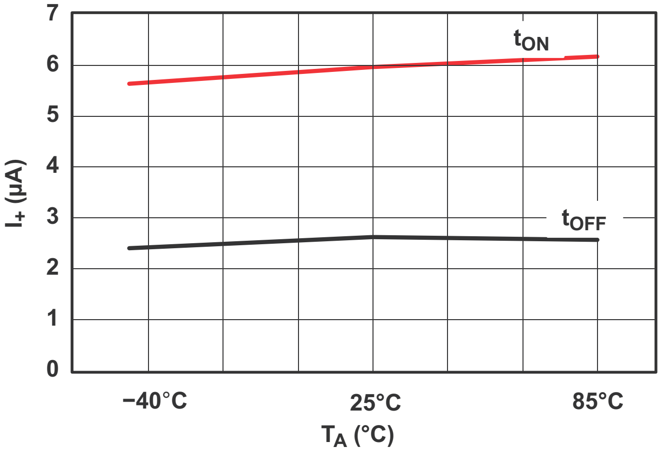


Figure 7. t_{ON} and t_{OFF} vs Temperature (V_+ = 5 V)

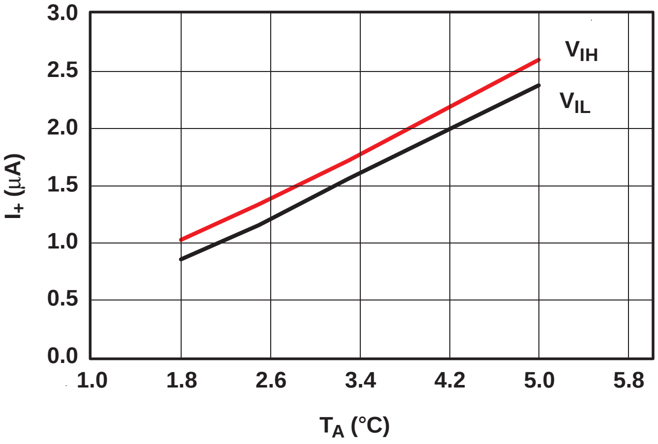


Figure 8. Logic-Level Threshold vs V_+

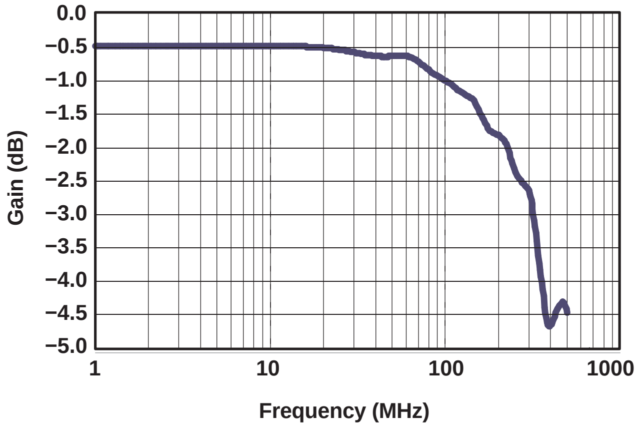


Figure 9. Bandwidth (Gain vs Frequency) (V_+ = 5 V)

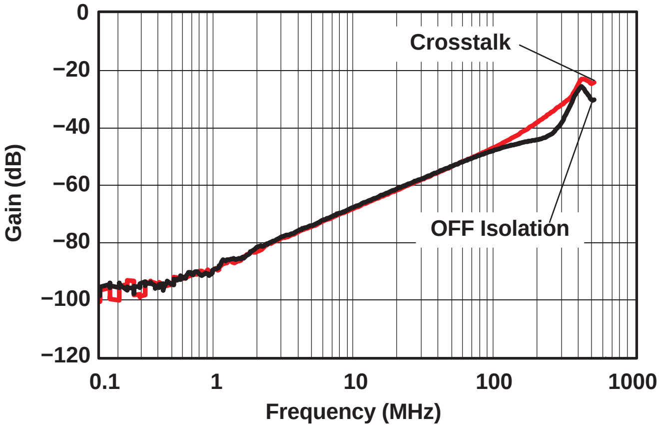


Figure 10. OFF Isolation (V_+ = 5 V)

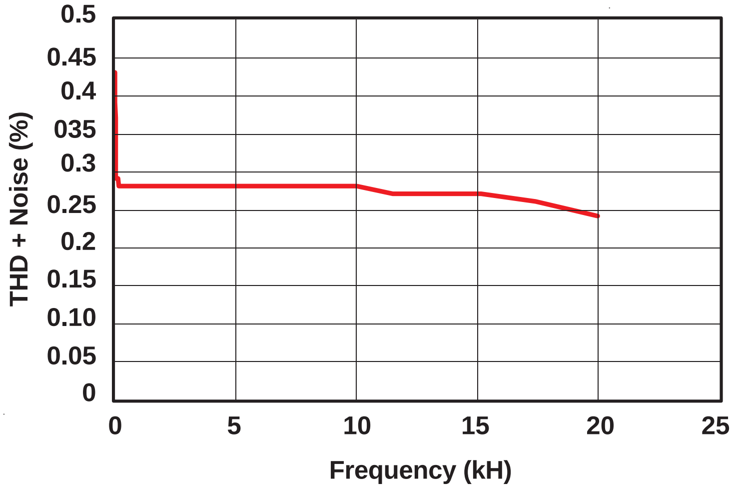


Figure 11. Total Harmonic Distortion vs Frequency

7 Parameter Measurement Information

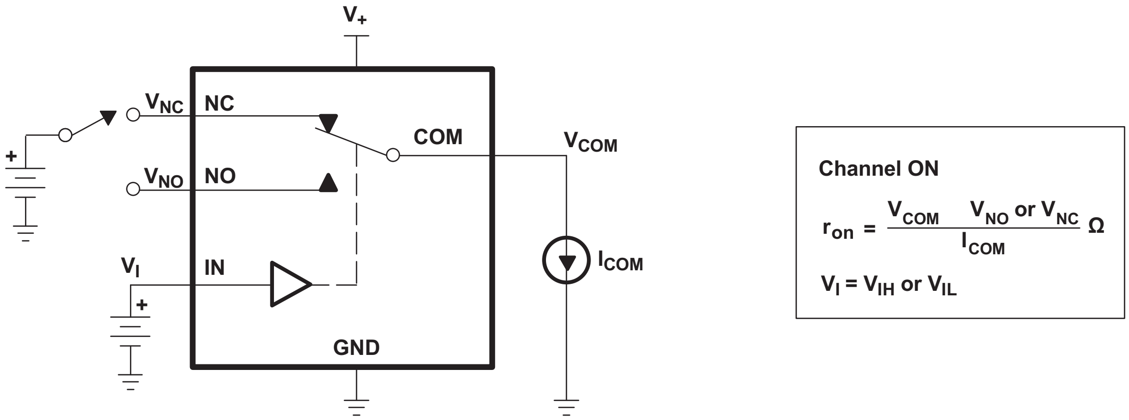


Figure 12. ON-State Resistance (r_{on})

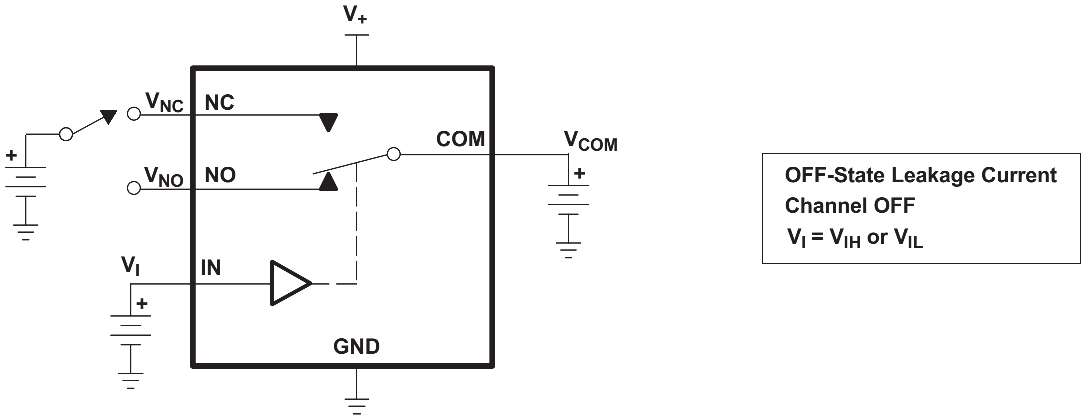


Figure 13. OFF-State Leakage Current ($I_{NC(OFF)}$, $I_{NO(OFF)}$)

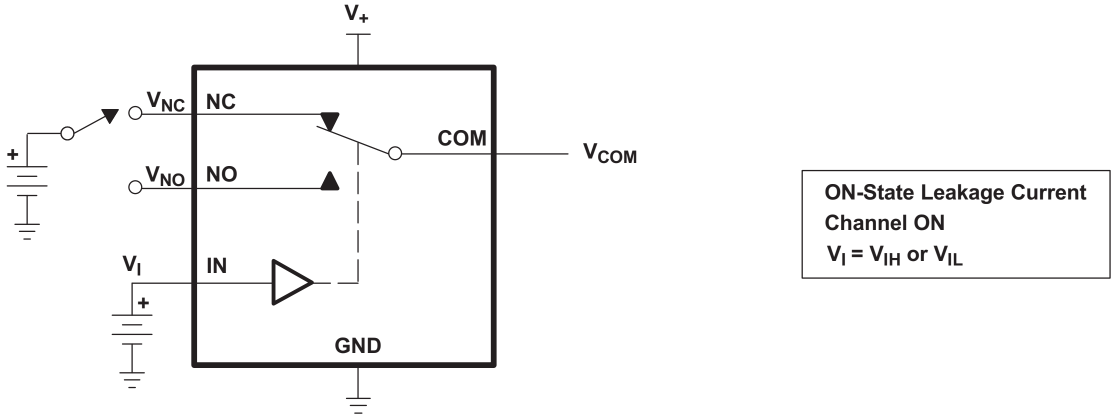


Figure 14. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

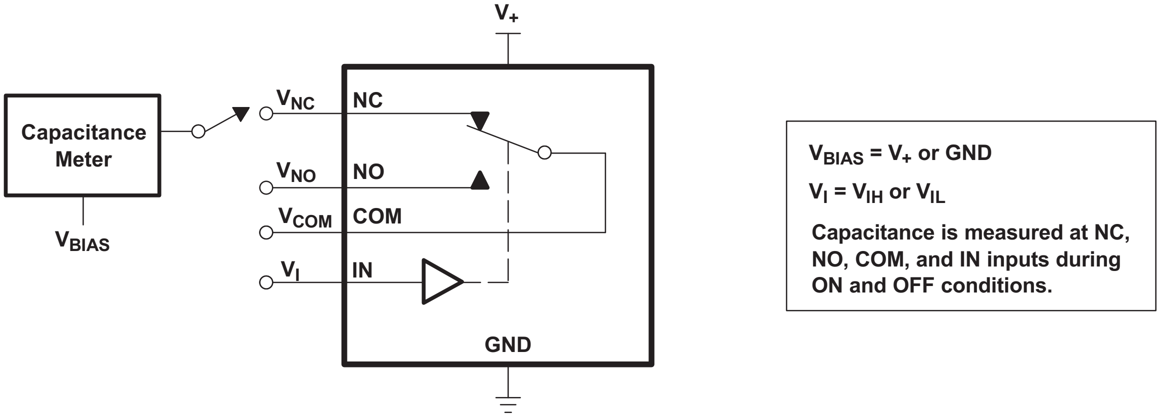
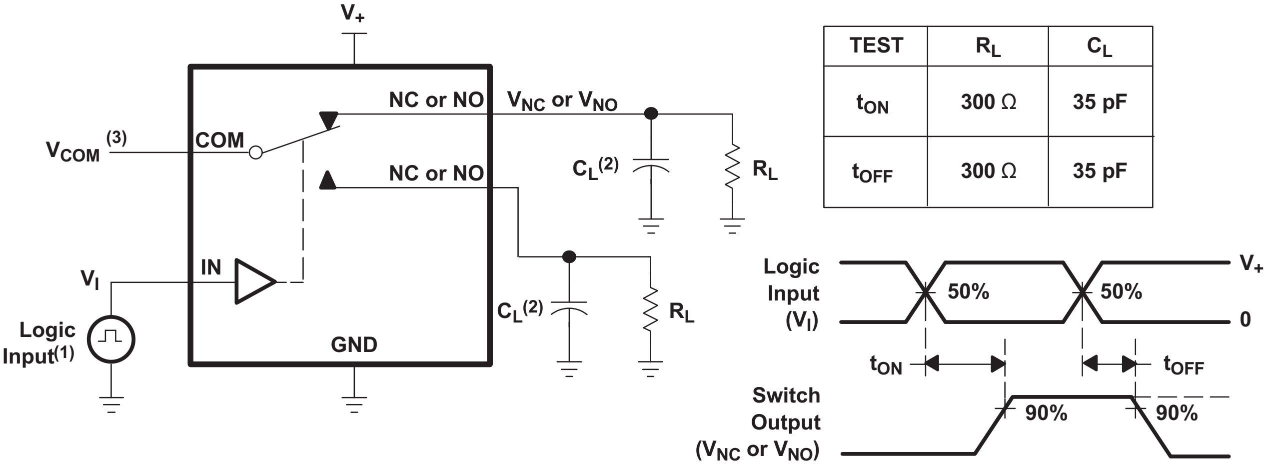


Figure 15. Capacitance (C_I, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)



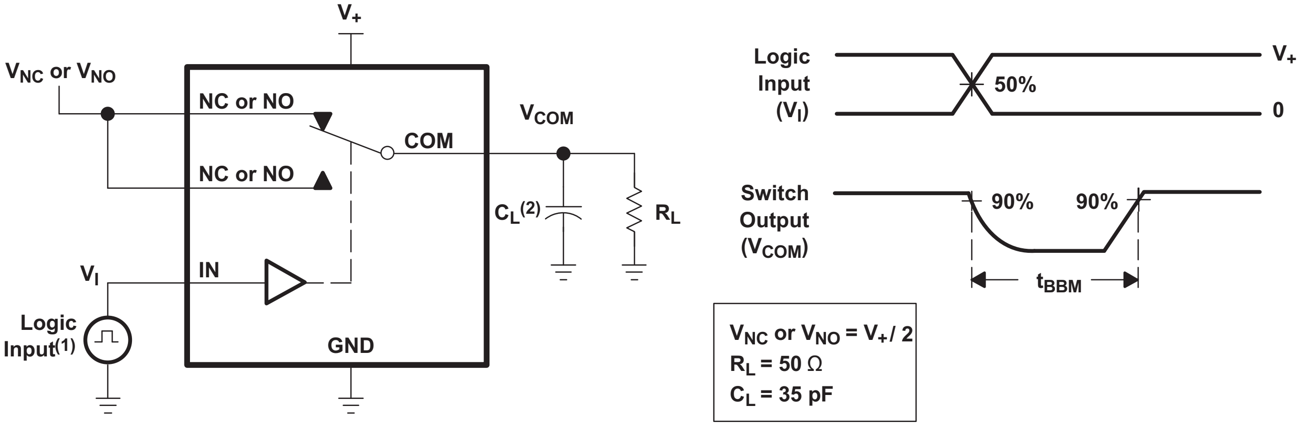
TEST	R_L	C_L
t_{ON}	300 Ω	35 pF
t_{OFF}	300 Ω	35 pF

(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

(3) See Electrical Characteristics for V_{COM}.

Figure 16. Turnon (t_{ON}) and Turnoff Time (t_{OFF})



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 17. Break-Before-Make Time (t_{BBM})

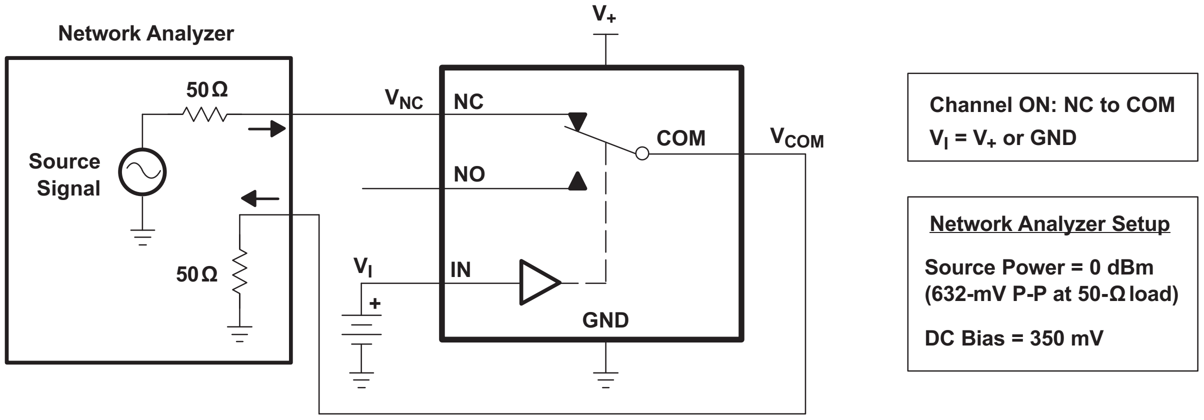


Figure 18. Bandwidth (BW)

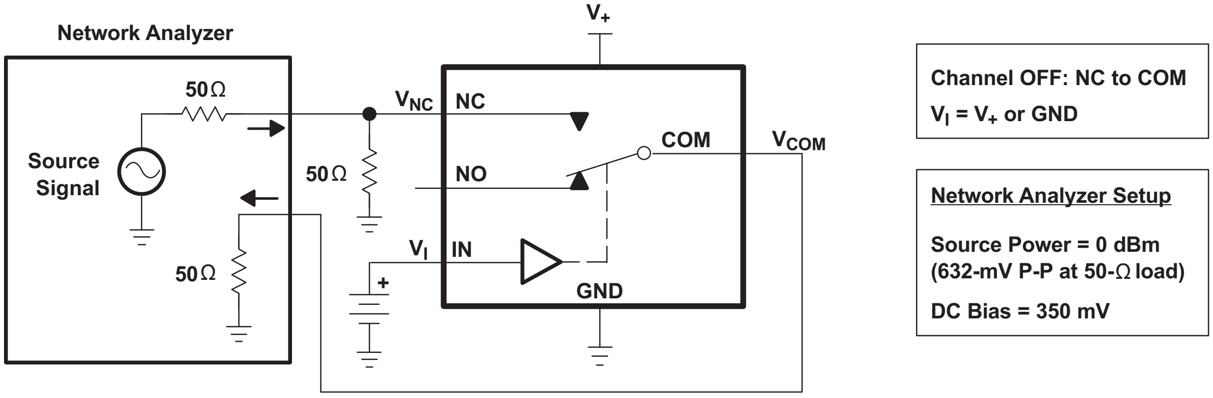


Figure 19. OFF Isolation (O_{ISO})

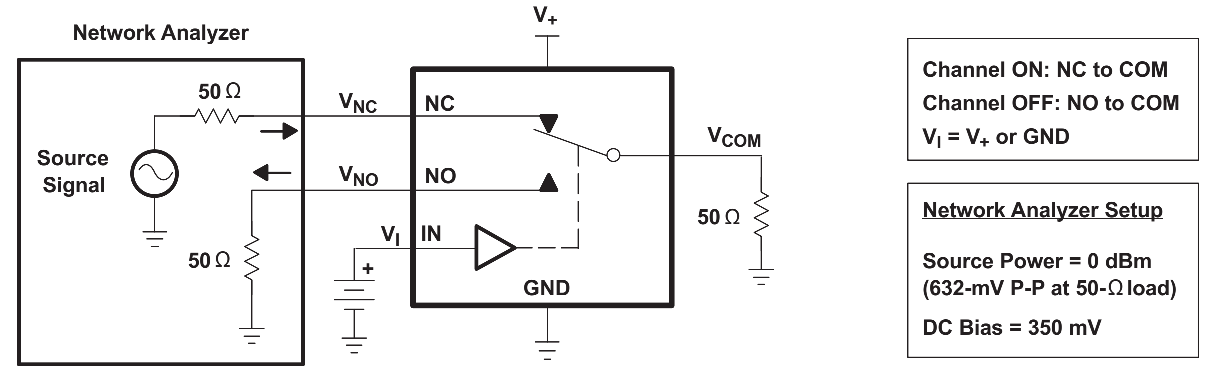
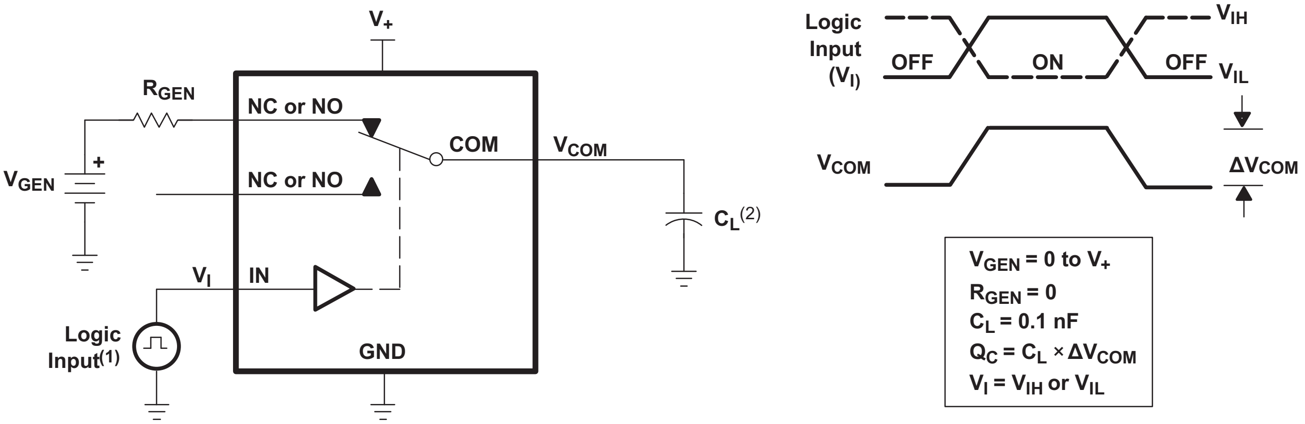


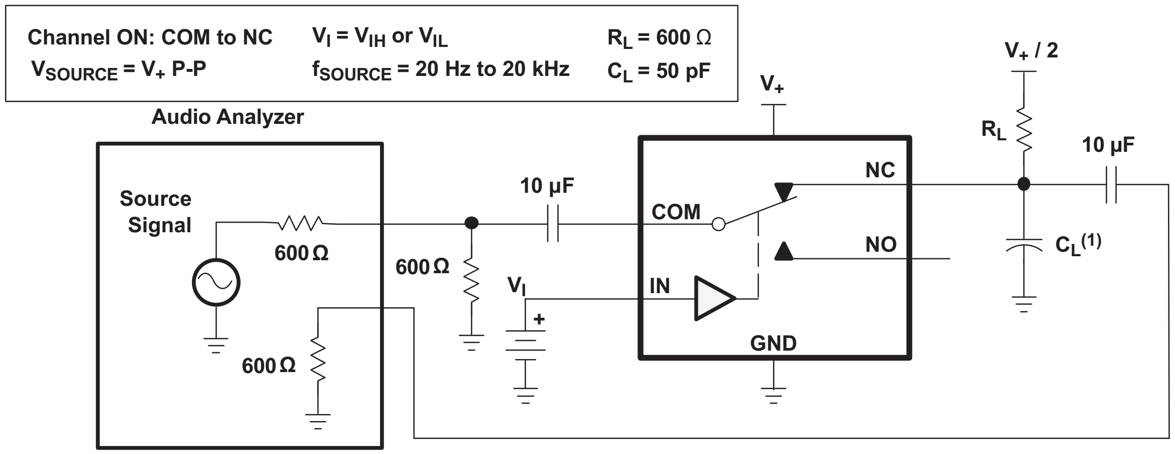
Figure 20. Crosstalk (X_{TALK})



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 21. Charge Injection (Q_C)



(1) C_L includes probe and jig capacitance.

Figure 22. Total Harmonic Distortion (THD)

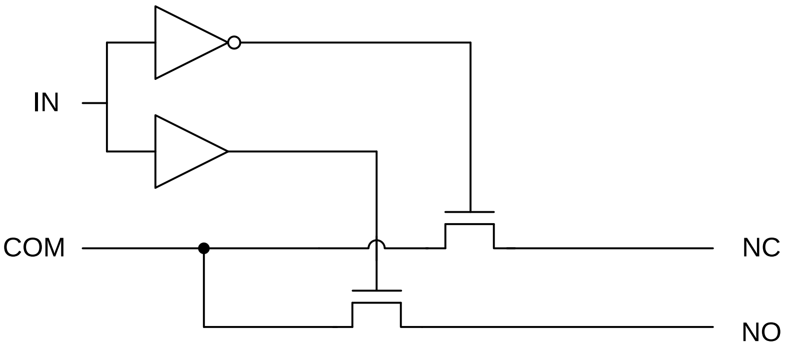
8 Detailed Description

8.1 Overview

The TS5A3157 is a single-pole-double-throw (SPDT) solid-state analog switch. The TS5A3157, like all analog switches, is bidirectional. When powered on, each COM pin is connected to the NC pin. For this device, NC stands for *normally closed* and NO stands for *normally open*. If IN is low, COM is connected to NC. If IN is high, COM is connected to NO.

The TS5A3157 is a break-before-make switch. This means that during switching, a connection is broken before a new connection is established. The NC and NO pins are never connected to each other.

8.2 Functional Block Diagram



8.3 Feature Description

The low ON-state resistance, ON-state resistance matching, and charge injection in the TS5A3157 make this switch an excellent choice for analog signals that require minimal distortion. In addition, the low THD allows audio signals to be preserved more clearly as they pass through the device.

The 1.65-V to 5.5-V operation allows compatibility with more logic levels, and the bidirectional I/Os can pass analog signals from 0 V to V_+ with low distortion. The control inputs are 5-V tolerant, allowing control signals to be present without V_{CC}.

8.4 Device Functional Modes

Table 1. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS5A3157 can be used in a variety of customer systems. The TS5A3157 can be used anywhere multiple analog or digital signals must be selected to pass across a single line.

9.2 Typical Application

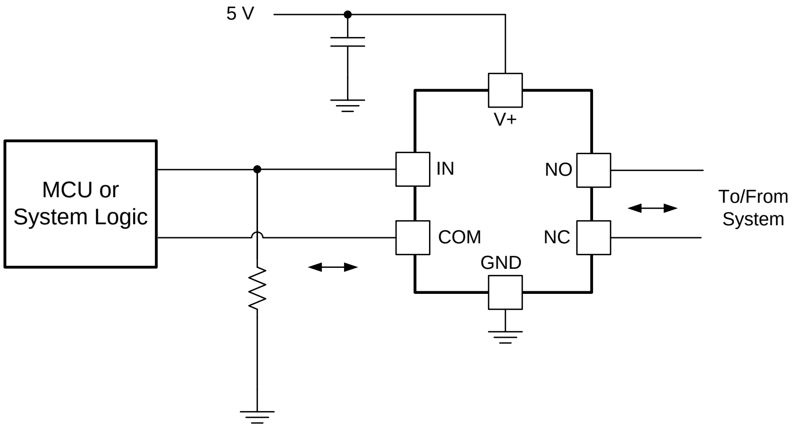


Figure 23. System Schematic for TS5A3157

9.2.1 Design Requirements

In this particular application, V_+ was 1.8 V, although V_+ is allowed to be any voltage specified in *Recommended Operating Conditions*. A decoupling capacitor is recommended on the V+ pin. See *Power Supply Recommendations* for more details.

9.2.2 Detailed Design Procedure

In this application, IN is, by default, pulled low to GND. Choose the resistor size based on the current driving strength of the GPIO, the desired power consumption, and the switching frequency (if applicable). If the GPIO is open-drain, use pullup resistors instead.

Typical Application (continued)

9.2.3 Application Curve

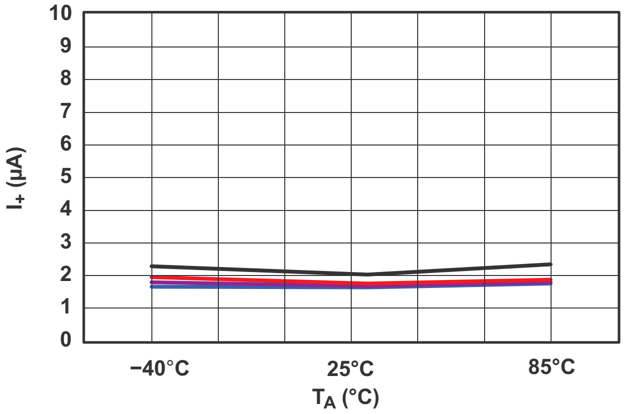


Figure 24. Power-Supply Current vs Temperature ($V_+ = 5$ V)

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01-μF or 0.022-μF capacitor is recommended for each V_{CC} because the VCC pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-μF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Below figure shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

Unused switch I/Os, such as NO, NC, and COM, can be left floating or tied to GND. However, the IN pin must be driven high or low. Due to partial transistor turnon when control inputs are at threshold levels, floating control inputs can cause increased I_{CC} or unknown switch selection states.

11.2 Layout Example

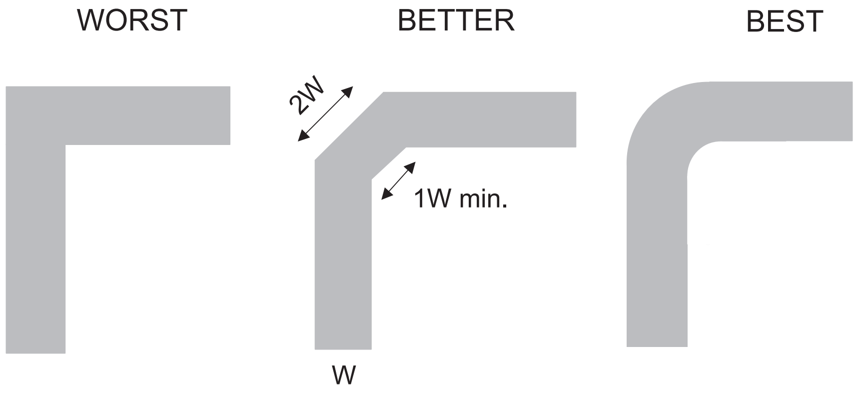


Figure 25. Trace Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

Table 2. Parameter Description

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NC}	Voltage at NC
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NC or COM and NO ports when the channel is ON
Δr_{on}	Difference of r_{on} between channels in a specific device
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Maximum input voltage for logic low for the control input (IN)
V_I	Voltage at the control input (IN)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN)
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning OFF.
t_{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance and ΔV_{COM} is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
C_I	Capacitance of control input (IN)
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency where the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of fundamental harmonic.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

- *Implications of Slow or Floating CMOS Inputs*, SCBA004

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A3157DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JC5R	Samples
TS5A3157DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JC5R	Samples
TS5A3157DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JC5 ~ JCF ~ JCR)	Samples
TS5A3157DCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JC5 ~ JCF ~ JCR)	Samples
TS5A3157DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JC5 ~ JCF ~ JCR)	Samples
TS5A3157YZPR	ACTIVE	DSBGA	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(JC7 ~ JCN)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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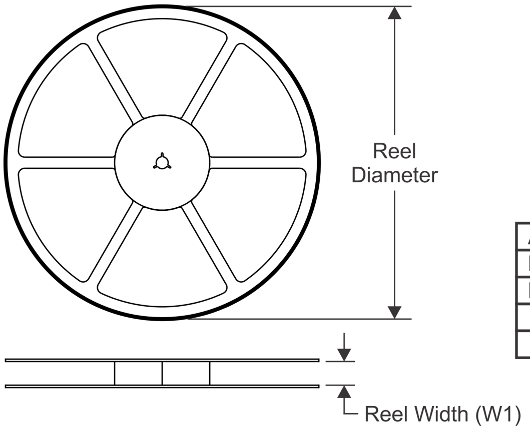
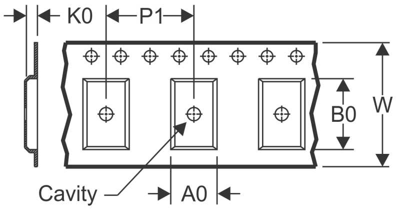
TAPE AND REEL INFORMATION

REEL DIMENSIONS

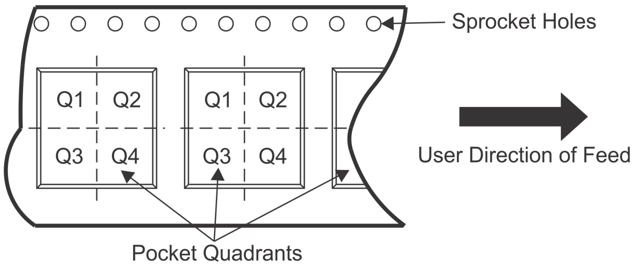


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

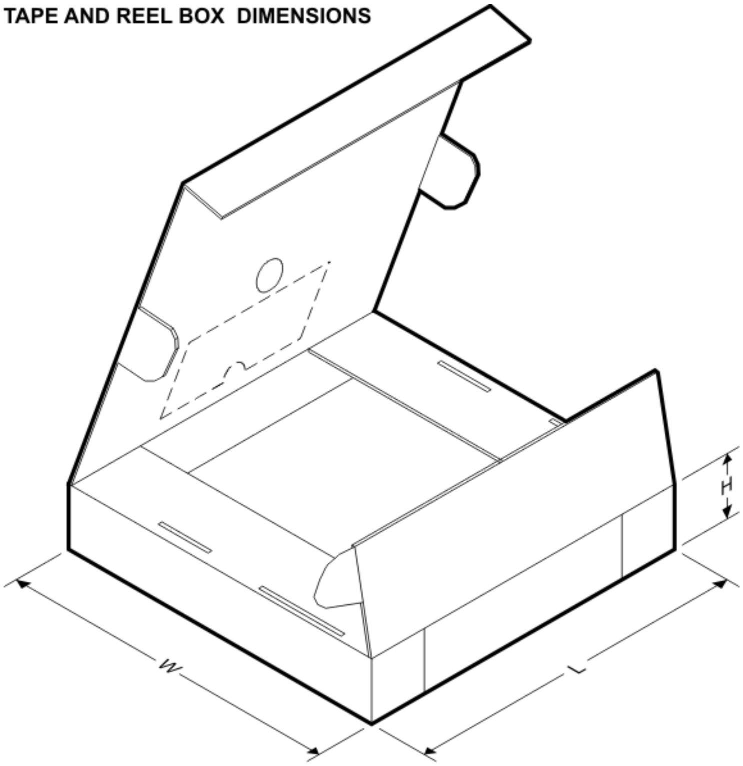
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3157DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TS5A3157DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TS5A3157DCKR	SC70	DCK	6	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
TS5A3157YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

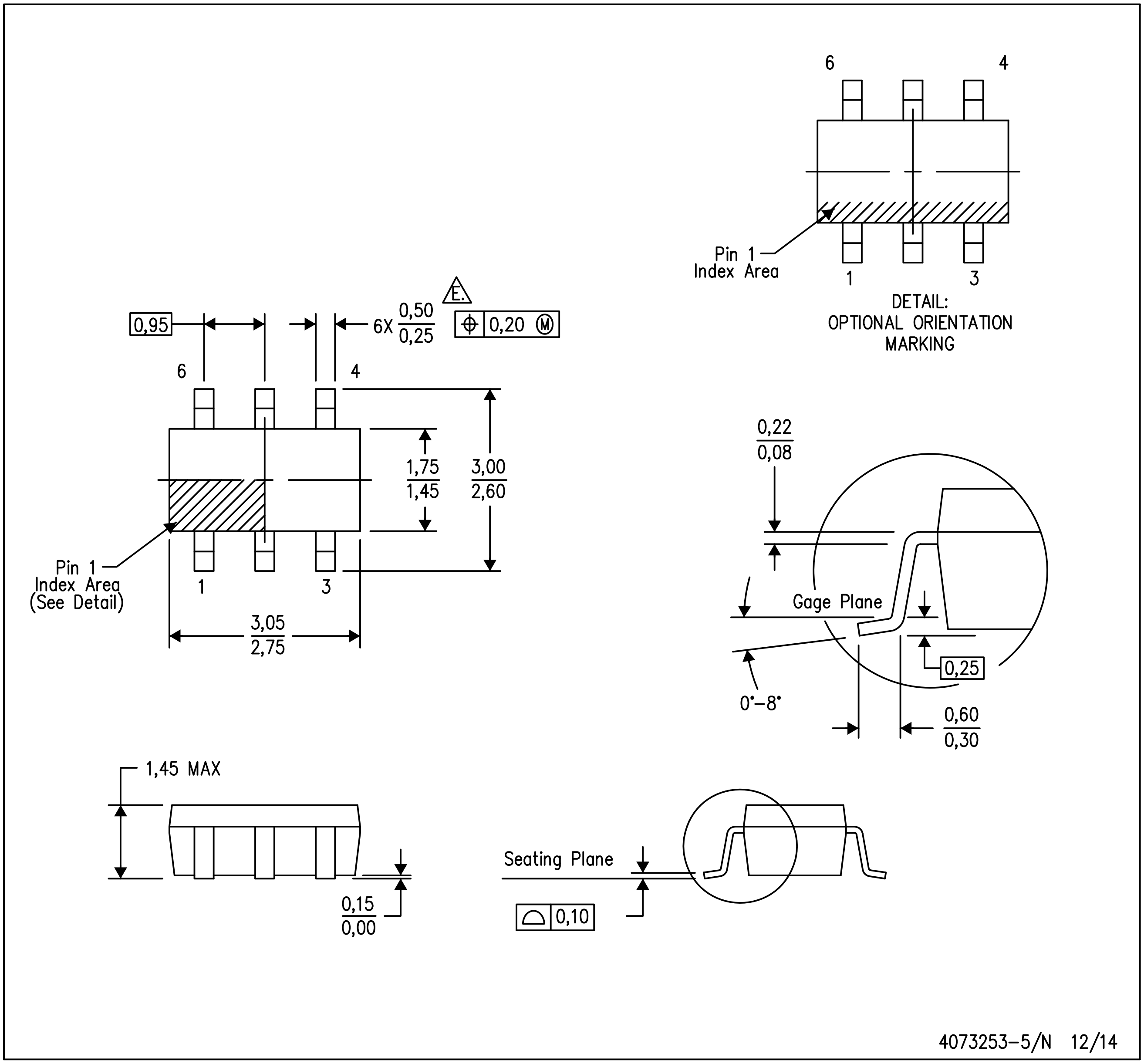
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

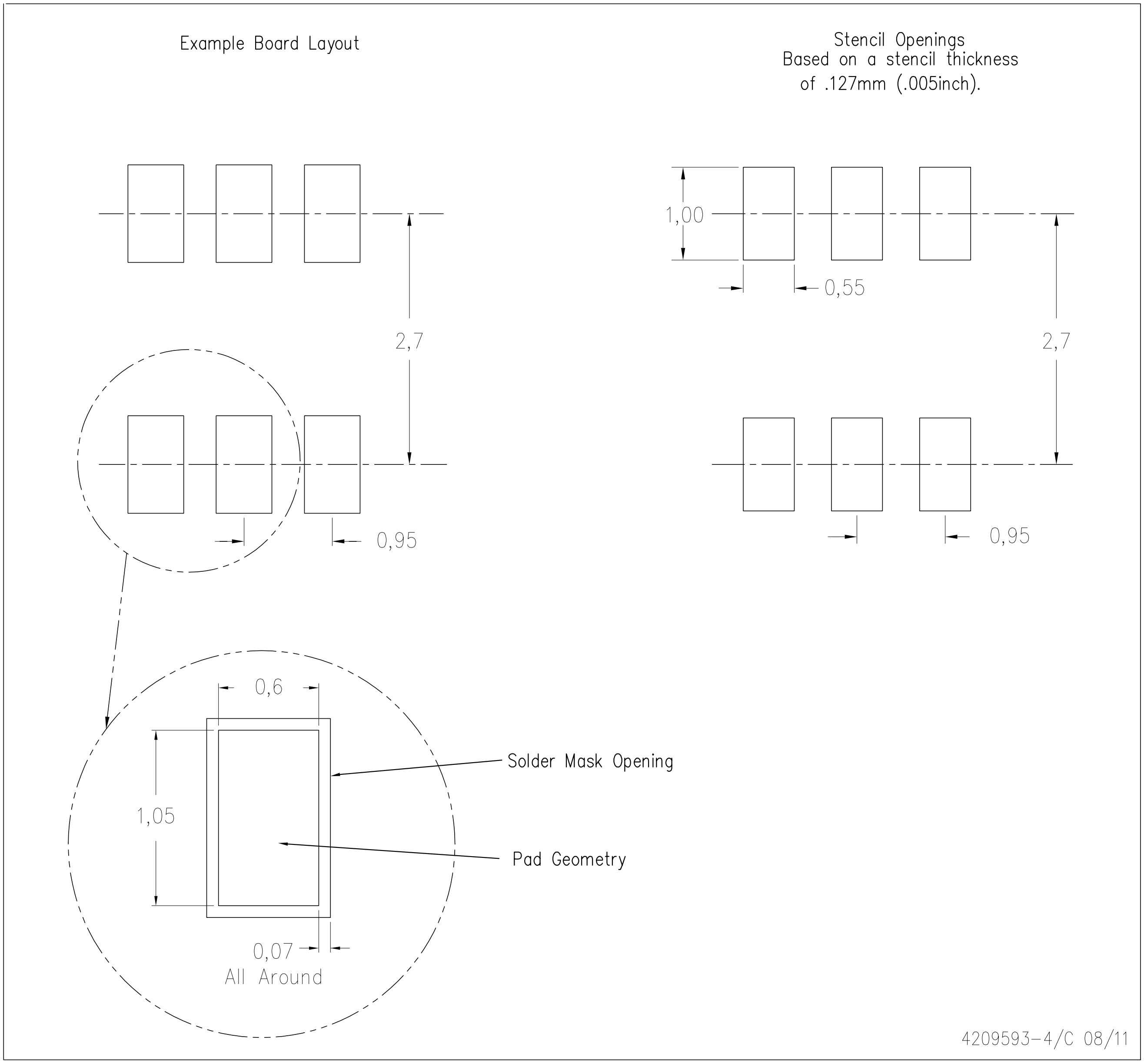
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3157DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
TS5A3157DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
TS5A3157DCKR	SC70	DCK	6	3000	338.0	343.0	30.0
TS5A3157YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



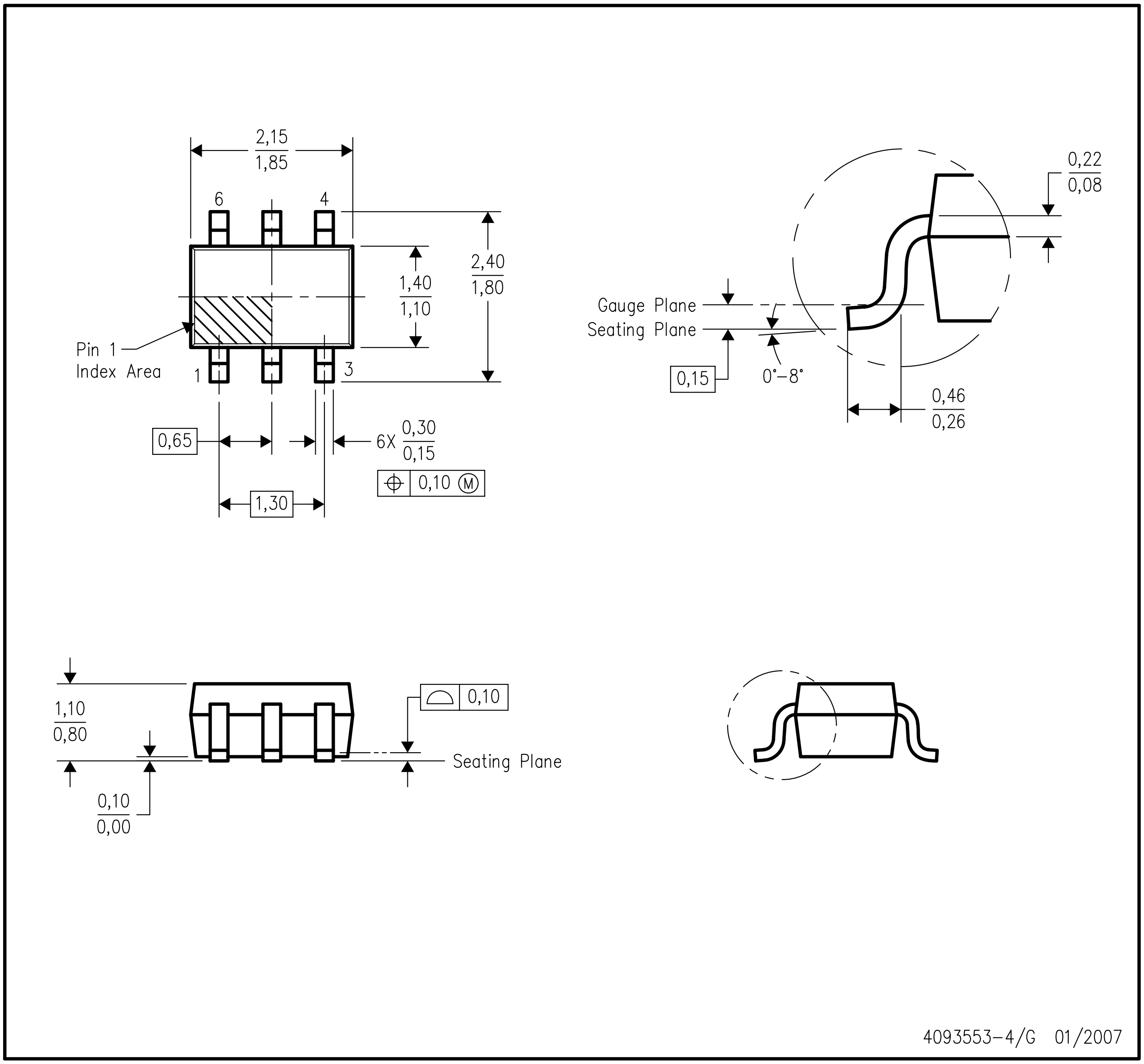
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

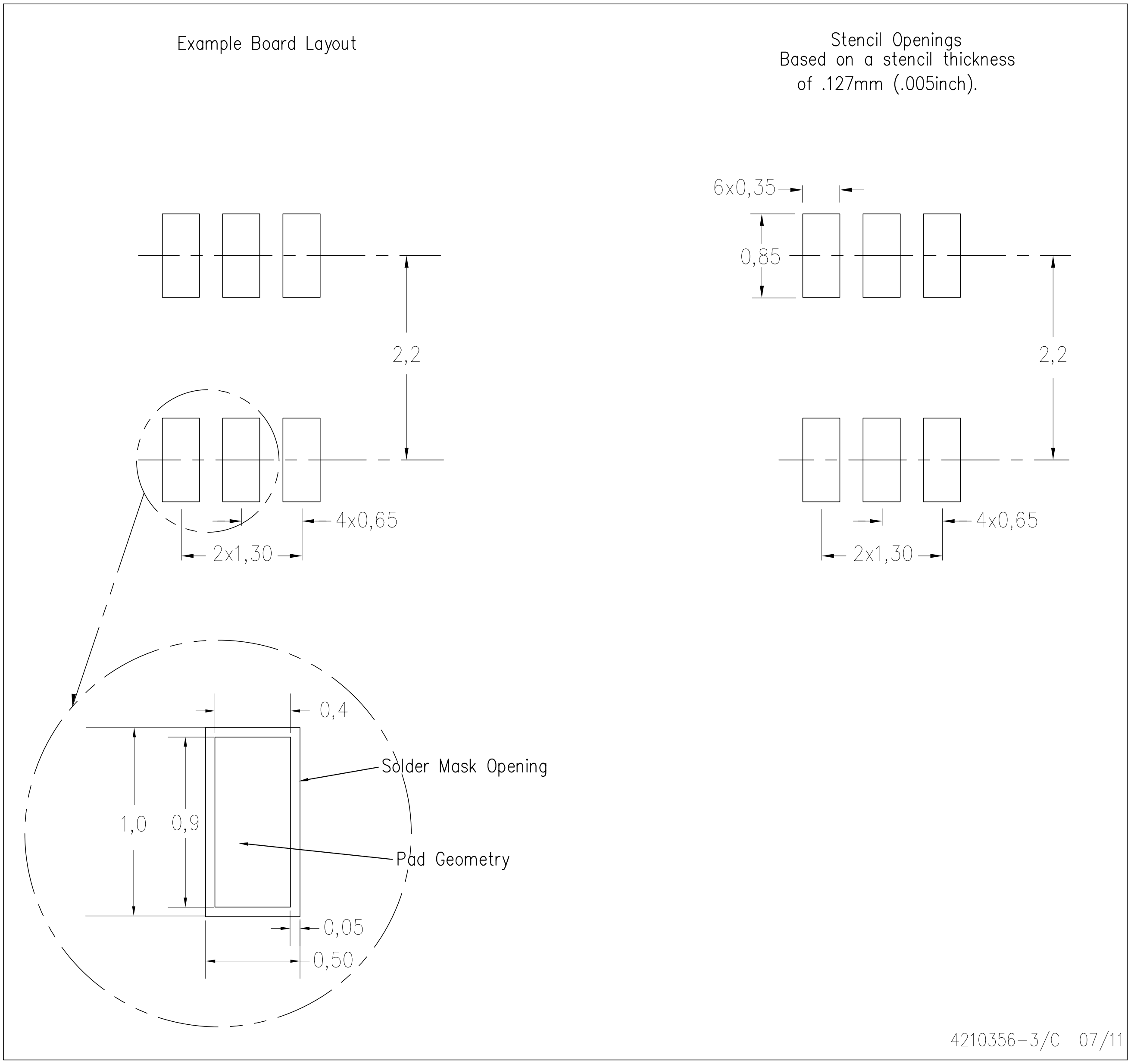
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



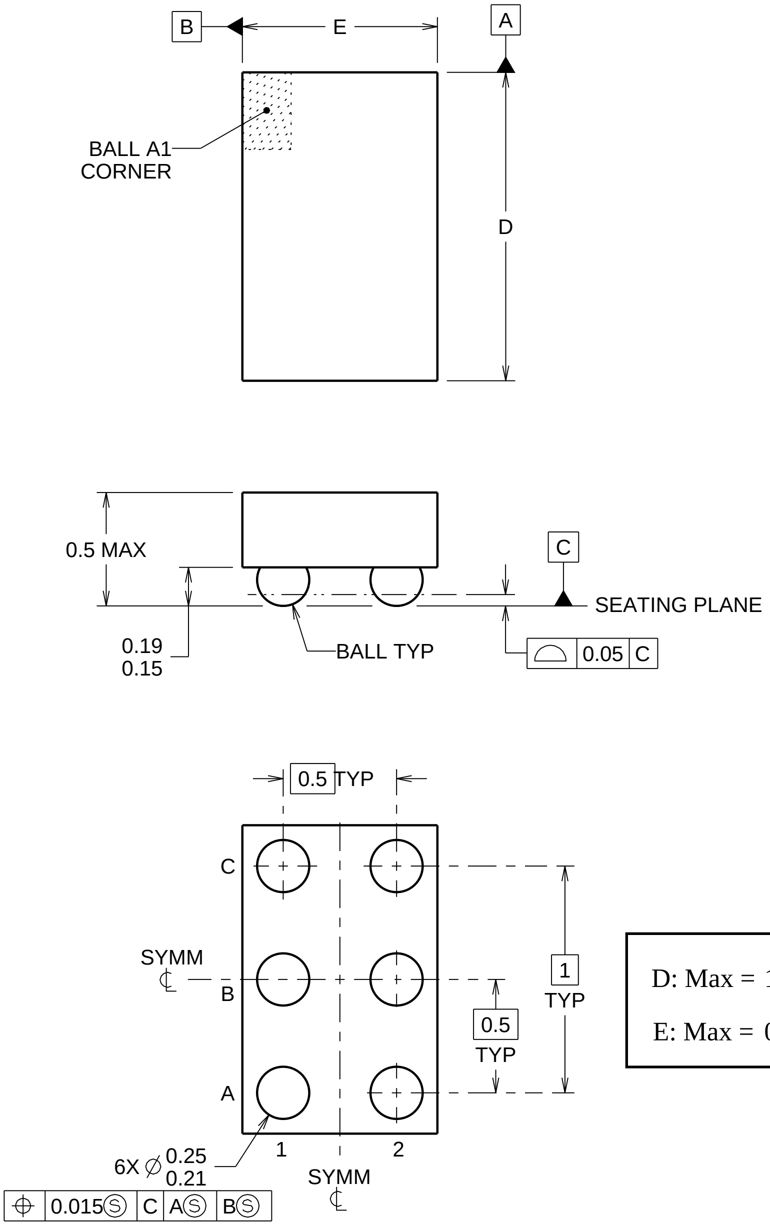
4093553-4/G 01/2007

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.



D: Max = 1.418 mm, Min =1.358 mm

E: Max = 0.918 mm, Min =0.858 mm

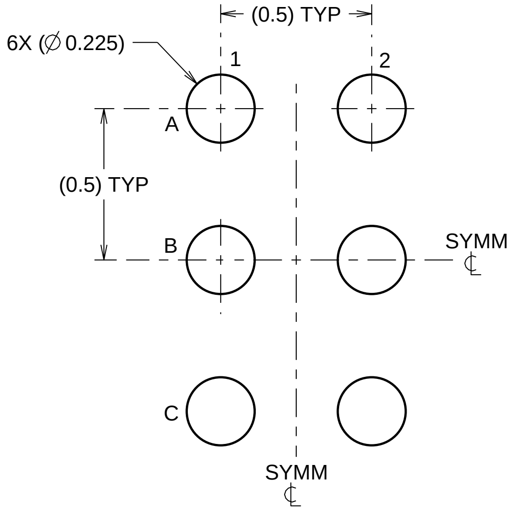
4219524/A 06/2014

NOTES:

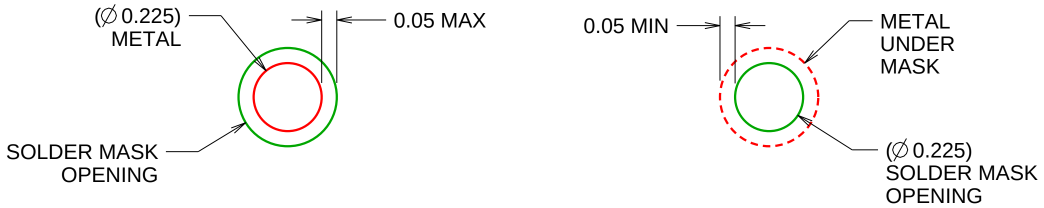
NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
SCALE:40X



NON-SOLDER MASK
DEFINED
(PREFERRED)

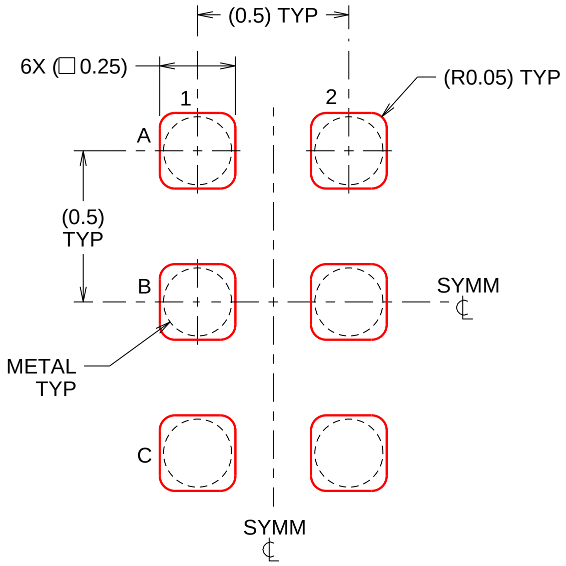
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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